

IBM Customer Engineering
Handbook

Printed in U.S.A.

223-2640-2

7040-7044 Data Processing Systems

IBM

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, N.Y. 10601



**Customer Engineering Handbook
7040-7044 Data Processing Systems**

SAFETY

Ungrounded oscilloscopes are dangerous. Voltages that are not referenced to ground are safely measured by using the Tektronix type CA plug-in unit available for all Tektronix 500 series oscilloscopes except the Tektronix 561A oscilloscope. The add feature of the type CA plug-in unit is incorporated in the type 3A1 plug-in unit for the Tektronix 561A oscilloscope. The add feature is explained in the IBM Tektronix Oscilloscopes CE Manual of Instruction, Form 223-6725-4, available from Stationery Stores, Endwell, New York.

Pressing the master power disconnect key does not remove 24 vac from the console or power supply area. For your own personal safety, disconnect all power via the customer's wall switch before working in these areas.

Pressing the normal power off key does not remove power from the convenience outlets nor the -48 vdc from the power supply area or the console. For your own personal safety, disconnect all power via the customer's wall switch before working in these areas.

Your own personal safety cannot be overemphasized. Make it a daily practice to work safely. Be familiar with safety practices listed on IBM Form 124-0082. Is your installation a safe place to work?

Are you working alone?

Are you wearing your safety glasses?

Did you turn off the power to replace that fuse?

Did you turn off the power to replace that SMS card?

Did you discharge the capacitors when you worked on that dc power supply?

Did you replace all of the safety covers?

MINOR REVISION (May 1964)

This edition, Form 223-2640-2, is a minor revision and does not obsolete any of the previous printings. This book reflects the latest information generated to assist Customer Engineers in maintaining the 7040 and 7044 Data Processing Systems. Many of the additions result from requests made by Customer Engineers on the postpaid comment card supplied in the back of each book.

Copies of this and other IBM publications can be obtained through IBM Branch Offices.

Address comments concerning the content of this publication to: IBM Corporation, CE Manuals, Dept. B95, PO Box 390, Poughkeepsie, New York 12602.

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7040-7044 CUSTOMER ENGINEERING MANUALS
March 11, 1964

All of these manuals are stocked in Endwell Stationery Stores.

CEIM or CEIR are combination Instruction-Maintenance Manuals.

CEMI is a CE Manual of Instruction.

CEMM or CERM are CE Maintenance Manuals.

ISD are Instructional Systems Diagrams.

FORM	MACHINE	NAME
223-2640	7040-7044	HANDBOOK
R23-2659	7040-7044	CPU LOGIC 01AGRAMS CERM
R23-2651	7040-7044	CENTRAL PROCESSING UNIT CEMI
223-2753	7040-7044	TRAPPING CEMM
223-2644	7040-7044	CHANNEL A CEMM
223-2652	7040-7044	CHANNEL A CEMI
223-2712	7040-7044	CHANNEL B-E CEMM
223-2755	7040-7044	CHANNEL B-E CEMI
R23-2680	7040-7044	POWER SUPPLIES CEIR
223-2593	7106	CORE STORAGE CEMI
R23-2645	7107	CORE STORAGE CERM
R23-2573	7107	CORE STORAGE CEMI
* 223-2618	0000	DDTL COMPONENT CIRCUITS CEMI
* 225-6747B	0000	SMS POWER SUPPLY CEMI
* 223-6783	0000	TRANSISTOR THEORY AND APP CEMI
* 223-6889	0000	TRANSISTOR COMPONENT CIRCUITS CEMI
* 223-6900	0000	STANDARD MODULAR SYSTEM CEIR
* 223-2509	0729	TAPE UNIT NOR-RELAY 1SD
* 223-6868	0729	TAPE UNIT M2, 3, AND 4 CERM
* 223-6988	0729	NOR TAPE CEIR
* 225-1726	0731	INPUT-OUTPUT PRINTER CERM
* 225-6595	0731	INPUT-OUTPUT PRINTER CEIR
* 223-6954	0000-1009	SYNCHRONOUS TRANS-REC M1 AND 2 CEMI
* 225-6561	1009	DATA TRANSMISSION UNIT CERM
* 225-6560	1009	DATA TRANSMISSION UNIT CEMI
* 227-5545	1011	PAPER TAPE READER CERM
* 227-5546	1011	PAPER TAPE READER CEMI
* 225-6583	1014	REMOTE INQUIRY UNIT CEIR
* 227-5582	1301	DISK STORAGE CEMI
* 227-5582	1301	DISK STORAGE CERM
* 225-6487	1401	DATA PROCESSING SYSTEM CERM
* 225-6540	1401	DATA PROCESSING SYSTEM CEMI
* 225-6541	1401	DPS OPTIONAL FEATURES CEMI
* 225-0002	1402	CARD REAO-PUNCH CEIR
* 225-6492	1403	PRINTER CEMI
* 225-6493	1403	PRINTER CERM
* 223-2554	1414M1	1-0 SYNC M1, 2, AND 7 CEIR
* 223-2590	1414M3	1-0 SYNC M3, 4, 6, AND B CEIR
* 223-2609	1414M1	1-0 SYNC M1, 2, AND 7 1SD
* 223-2630	1414M3	1-0 SYNC M3, 4, 6, AND 8 1SD
* 227-5612	1622	CARD READER-PUNCH 1SD
* 227-5806	1622	CARD READER-PUNCH CEMI
* 227-5715	1622	CARD READER-PUNCH CERM
* 223-6930	7330	MAGNETIC TAPE UNIT 150
* 223-6943	7330	MAGNETIC TAPE UNIT CEMI
* 223-6967	7330	MAGNETIC TAPE UNIT CERM
* 222-2766	7631	FILE CONTROL CEIR
* 223-2533	7750	INTRODUCTION TO THE PTC CEMI
* 223-2540	7750	PROCESS STOR AND CTRL STOR CEMI
* 223-2544	7750	AAQAPTER AND CHANNEL WORD CEMI
* 223-2570	7750	PROCESS CONTROL CEMI
* 223-2579	7750	POWER SUPPLY AND DISTRIBUTION CEMI
* 223-2623	7750	PROCESS CONTROL CERM
* 223-2653	7750	COMMUNICATIONS INPUT-OUTPUT CERM
* 223-2654	7750	POWER SUPPLY AND STORAGE CERM

* THESE MANUALS ARE NOT PREPARED EXCLUSIVELY FOR THE
7040-7044 SYSTEMS.

R FORM NUMBERS ARE PRELIMINARY EDITIONS.

Z FORM NUMBERS ARE IBM CONFIDENTIAL.

A 7040-7044 CUSTOMER REFERENCE MANUAL BIBLIOGRAPHY,
FORM A2B-6288, IS AVAILABLE FROM STATIONERY STORES,
ENDWELL, NEW YORK.

0	1	2	3	4	5
S 5 6	11 12	17 18	23 24	29 30	35

B	A	8	4	2	1
S	1	2	3	4	5

Alphomeric Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
S	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

S	2	1	4	2	1
S	1	2	3	4	5

Numeric Word (Octal)

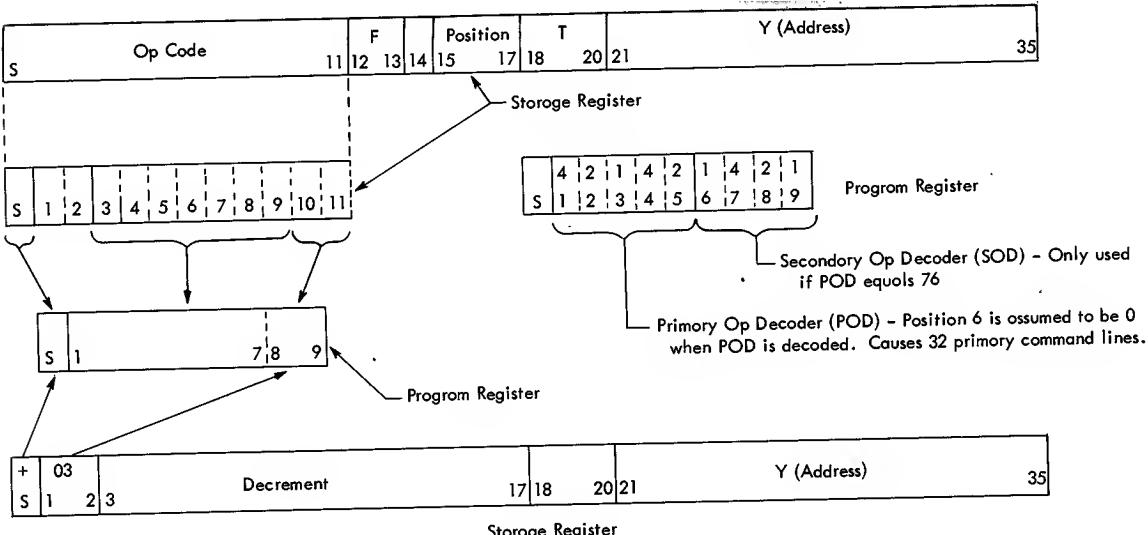
0	1	Characteristic	8	9
---	---	----------------	---	---

Fraction

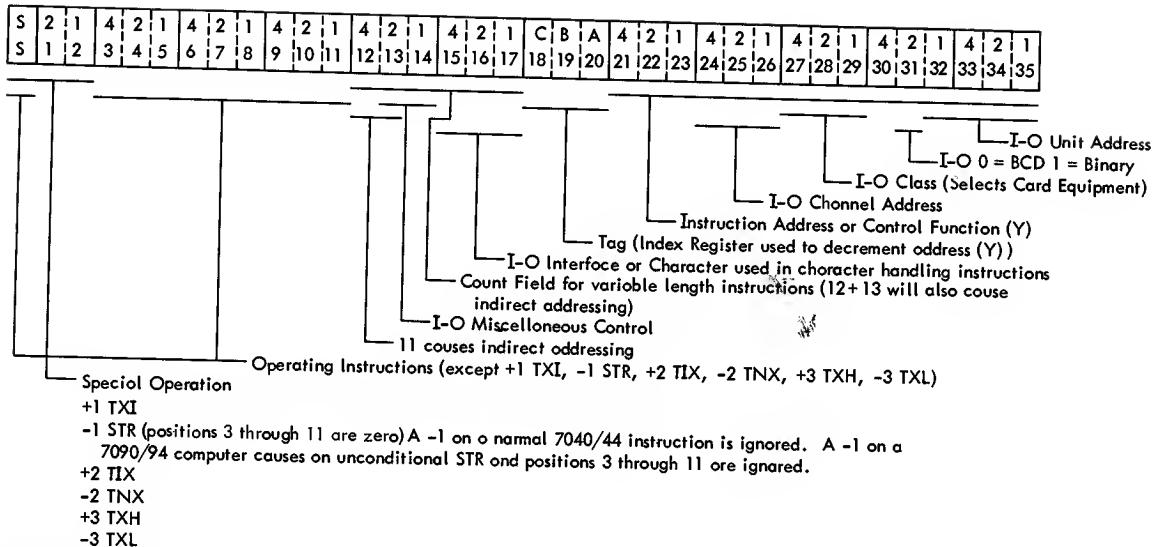
35

Floating Point Word

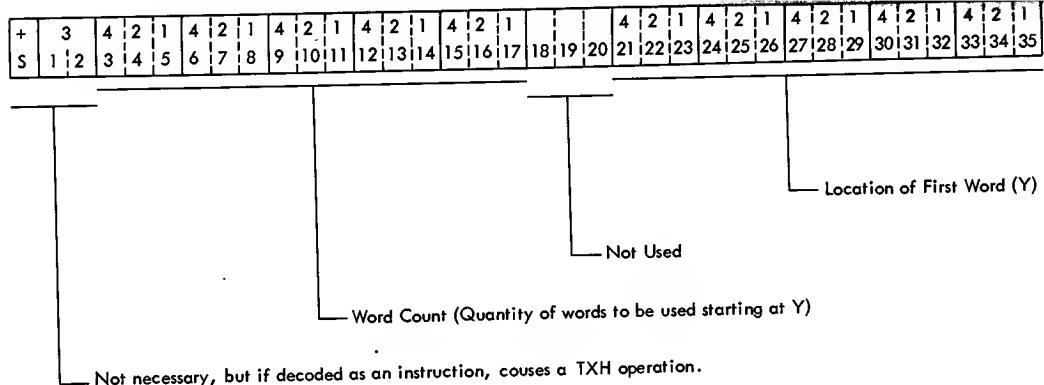
7040/7044 Data Word Format



Program Register



7040/44 Instruction Format



IORD Word Format

CHARACTER CODING AND TRANSLATION

CORE STORAGE BYTE	TAPE	OTHER	TYPEWRITER		TYPEWRITER	
			REPORT WITH GRAPHICS		PROGRAMMING WITH GRAPHICS	
			BCD	BCD	BCD	BINARY
000 000	0 000 000	1 001 010	0	Blank	0	Blank
000 001	1 000 001	0 000 001	1	1	1	1
000 010	1 000 010	0 000 010	2	2	2	2
000 011	0 000 011	1 000 011	3	3	3	3
000 100	1 000 100	0 000 100	4	4	4	4
000 101	0 000 101	1 000 101	5	5	5	5
000 110	0 000 110	1 000 110	6	6	6	6
000 111	1 000 111	0 000 111	7	7	7	7
001 000	1 001 000	0 001 000	8	8	8	8
001 001	0 001 001	1 001 001	9	9	9	9
001 010	0 001 010*	0 001 000	0	0	0	0
001 011	1 001 011	0 001 011	#	#	=	=
001 100	0 001 100	1 001 100	0	0	0	0
001 101	1 001 101	0 001 101	:	:	:	:
001 110	1 001 110	0 001 110	>	>	>	>
001 111	0 001 111	1 001 111	✓ TM	✓	✓	✓
010 000	0 110 000	1 110 000	6	6	+	+
010 001	1 110 001	0 110 001	A	/	A	/
010 010	1 110 010	0 110 010	B	S	B	S
010 011	0 110 011	1 110 011	C	T	C	T
010 100	1 110 100	0 110 100	0	U	0	U
010 101	0 110 101	1 110 101	E	V	E	V
010 110	0 110 110	1 110 110	F	W	F	W
010 111	1 110 111	0 110 111	G	X	G	X
011 000	1 111 000	0 111 000	H	Y	H	Y
011 001	0 111 001	1 111 001	I	Z	I	Z
011 010	0 111 010	1 111 010	?	±	?	±
011 011	1 111 011	0 111 011	,	,	,	,
011 100	0 111 100	1 111 100	□	%)	(
011 101	1 111 101	0 111 101	C	~	[~
011 110	1 111 110	0 111 110	<	\	<	~
011 111	0 111 111	1 111 111	‡ GM	#+	‡	#+
100 000	1 100 000	0 100 000	-	-	-	-
100 001	0 100 001	1 100 001	J	J	J	J
100 010	0 100 010	1 100 010	K	K	K	K
100 011	1 100 011	0 100 011	L	L	L	L
100 100	0 100 100	1 100 100	M	M	M	M
100 101	1 100 101	0 100 101	N	N	N	N
100 110	0 100 110	0 100 110	O	O	O	O
100 111	0 100 111	1 100 111	P	P	P	P
101 000	0 101 000	1 101 000	Q	Q	Q	Q
101 001	1 101 001	0 101 001	R	R	R	R
101 010	0 101 010	1 101 010	!	!	!	!
101 011	0 101 011	1 101 011	\$	\$	\$	\$
101 100	1 101 100	0 101 100	•	•	•	•
101 101	0 101 101	1 101 101]]]]
101 110	0 101 110	1 101 110	:	:	:	:
101 111	0 101 111	0 101 111	Δ	Δ	Δ	Δ
110 000	1 000 000	Blank	&	Blank	+	Blank
110 001	0 000 001	1 000 001	/	A	/	A
110 010	0 000 010	1 000 010	S	B	S	B
110 011	1 000 011	0 000 011	T	C	T	C
110 100	0 000 100	1 000 100	U	O	U	O
110 101	1 000 101	0 000 101	V	E	V	E
110 110	0 000 110	1 000 110	W	F	W	F
110 111	0 000 111	1 000 111	X	G	X	G
111 000	0 011 000	1 011 000	Y	H	Y	H
111 001	1 011 001	0 011 001	Z	I	Z	I
111 010	0 011 010	1 011 010	‡ RM	?	‡	?
111 011	0 011 011	1 011 011	,	,	,	,
111 100	1 011 100	0 011 100	%	~	()
111 101	0 011 101	1 011 101	□	~	~	~
111 110	0 011 110	0 011 110	<	\	<	~
111 111	1 011 111	0 011 111	++	‡	++	‡

* CORE STORAGE = 000 000 on READ

PRINTER		PRINTER		READ - PUNCH	
"A" CHAIN		"H" CHAIN		IBM CARD CODE	
BCD	BINARY	BCD	BINARY	BCD	
0	Blank	0	Blank	0	
1	1	1	1	1	
2	2	2	2	2	
3	3	3	3	3	
4	4	4	4	4	
5	5	5	5	5	
6	6	6	6	6	
7	7	7	7	7	
8	8	8	8	8	
9	9	9	9	9	
‡	‡	‡	‡	‡	
#	#	=	=	=	
0	0	-	-	-	
Blank	Blank	Blank	Blank	Blank	
Blank	Blank	Blank	Blank	Blank	
Blank	Blank	Blank	Blank	Blank	
&	‡	+	‡	12	
A	S	A	S	12-1	
B	C	B	C	12-2	
C	T	C	T	12-3	
D	U	D	U	12-4	
E	V	E	V	12-5	
F	W	F	W	12-6	
G	X	G	X	12-7	
H	Y	H	Y	12-8	
I	Z	I	Z	12-9	
&	‡	+	‡	12-10	
‡	‡	‡	‡	12-11	
Blank	Blank	Blank	Blank	Blank	
Blank	Blank	Blank	Blank	Blank	
Blank	Blank	Blank	Blank	Blank	
-	-	-	-	-	
J	J	J	J	J	11-1
K	K	K	K	K	11-2
L	L	L	L	L	11-3
M	M	M	M	M	11-4
N	N	N	N	N	11-5
O	O	O	O	O	11-6
P	P	P	P	P	11-7
Q	Q	Q	Q	Q	11-8
R	R	R	R	R	11-9
—	—	—	—	—	11-0
‡	‡	‡	‡	‡	11-8-3
*	*	*	*	*	11-8-4
Blank	Blank	Blank	Blank	Blank	11-8-5
Blank	Blank	Blank	Blank	Blank	11-8-6
Blank	Blank	Blank	Blank	Blank	11-8-7
Blank	Blank	Blank	Blank	Blank	11-8-8
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Blank	Blank	Blank	Blank	Blank	11-8-10
Blank	Blank	Blank	Blank	Blank	11-8-11
Blank	Blank	Blank	Blank	Blank	11-8-12
Blank	Blank	Blank	Blank	Blank	11-8-13
Blank	Blank	Blank	Blank	Blank	11-8-14
Blank	Blank	Blank	Blank	Blank	11-8-15
Blank	Blank	Blank	Blank	Blank	11-8-16
T	C	T	C	T	0-3
U	D	U	D	U	0-4
V	E	V	E	V	0-5
W	F	W	F	F	0-6
X	G	X	G	G	0-7
Y	H	Y	H	H	0-8
Z	I	Z	I	I	0-9
‡	‡	‡	‡	‡	0-10
‡	‡	‡	‡	‡	0-11
‡	‡	‡	‡	‡	0-12
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Blank	Blank	Blank	Blank	Blank	0-21
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Blank	Blank	Blank	Blank	Blank	0-26
Blank	Blank	Blank	Blank	Blank	0-27
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Blank	Blank	Blank	Blank	Blank	0-32
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Blank	Blank	Blank	Blank	Blank	0-55
Blank	Blank	Blank	Blank	Blank	0-56
Blank	Blank	Blank	Blank	Blank	0-57
Blank	Blank	Blank	Blank	Blank	0-58
Blank	Blank	Blank	Blank	Blank	0-59
Blank	Blank	Blank	Blank	Blank	0-60
Blank	Blank	Blank	Blank	Blank	0-61
Blank	Blank	Blank	Blank	Blank	0-62
Blank	Blank	Blank	Blank	Blank	0-63
Blank	Blank	Blank	Blank	Blank	0-64
Blank	Blank	Blank	Blank	Blank	0-65
Blank	Blank	Blank	Blank	Blank	0-66
Blank	Blank	Blank	Blank	Blank	0-67
Blank	Blank	Blank	Blank	Blank	0-68
Blank	Blank	Blank	Blank	Blank	0-69
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Blank	Blank	Blank	Blank	Blank	0-71
Blank	Blank	Blank	Blank	Blank	0-72
Blank	Blank	Blank	Blank	Blank	0-73
Blank	Blank	Blank	Blank	Blank	0-74
Blank	Blank	Blank	Blank	Blank	0-75
Blank	Blank	Blank	Blank	Blank	0-76
Blank	Blank	Blank	Blank	Blank	0-77
Blank	Blank	Blank	Blank	Blank	0-78
Blank	Blank	Blank	Blank	Blank	0-79
Blank	Blank	Blank	Blank	Blank	0-80
Blank	Blank	Blank	Blank	Blank	0-81
Blank	Blank	Blank	Blank	Blank	0-82
Blank	Blank	Blank	Blank	Blank	0-83
Blank	Blank	Blank	Blank	Blank	0-84
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Blank	Blank	Blank	Blank	Blank	0-92
Blank	Blank	Blank	Blank	Blank	0-93
Blank	Blank	Blank	Blank	Blank	0-94
Blank	Blank	Blank	Blank	Blank	0-95
Blank	Blank	Blank	Blank	Blank	0-96
Blank	Blank	Blank	Blank	Blank	0-97
Blank	Blank	Blank	Blank	Blank	0-98
Blank	Blank	Blank	Blank	Blank	0-99
Blank	Blank	Blank	Blank	Blank	0-100

"9"=709, 7040, 7044,

7094.

Storage Code

"5"=705, 7080 and

BCD Magnetic

Tape Code

"14"=1401, 1410, 1414

Storage and

Buffer Code

"H"=Standard 64

INSTRUCTIONS

INPUT-OUTPUT DEVICE ADDRESS

BASIC INSTRUCTION SET - ALPHABETIC

SYM	NUMERIC	NAME	F	T
ACL	0361	ADD AND CARRY LOGICAL WORD	X	X
ADD	0400	ADD	X	X
ALS	0767	ACCUMULATOR LEFT SHIFT	X	X
ANA	-0320	AND TO ACCUMULATOR	X	X
ANR	-0321	ACCUMULATOR RIGHT SHIFT	X	X
BKR	0764	BACKSPACE RECORD	X	X
CAL	-0500	CLEAR AND ADD LOGICAL WORD	X	X
CAS	0340	COMPARE ACCUMULATOR WITH STORAGE	X	X
CHS	0766.00002	CHANGE SIGN	X	X
CIS	0502	CLEAR AND ADD	X	X
COM	0760.00006	COMPLEMENT MAGNITUDE	X	X
CTR	-1766.6BIT14	CONTROL SELECT (WRITE)	X	X
DIVP	0760.00012	DIVIDE CHECK TEST	X	X
DEMB	0524	DIVIDE OR PROCEED	X	X
ENK	0760.00004	ENTER KEYS	X	X
ETTA	-0760.01001	END OF TAPE TEST, CHANNEL A	X	X
ETTB	-0760.02001	END OF TAPE TEST, CHANNEL B	X	X
ETTC	-0760.03001	END OF TAPE TEST, CHANNEL C	X	X
ETTD	-0760.04001	END OF TAPE TEST, CHANNEL D	X	X
ETTE	-0760.05001	END OF TAPE TEST, CHANNEL E	X	X
HPR	0420	HALT AND PROCEED	X	X
ICT	-1760.00014	INHIBIT CHANNEL TRAPS	X	X
IOC	0760.00005	INPUT/OUTPUT CHECK TEST	X	X
ISG	-0760.00001	LOGICAL COMPARE ACCUMULATOR WITH STOR	X	X
LDQ	0560	LOAD MQ	X	X
LGL	-0763	LOGICAL LEFT SHIFT	X	X
LGR	-0765	LOGICAL RIGHT SHIFT	X	X
LLS	0563	LONG LEFT SHIFT	X	X
LRG	0565	LONG RIGHT SHIFT	X	X
MPY	0200	MULTIPLY	X	X
ORA	-0501	OR TO ACCUMULATOR	X	X
PBT	-0760.00001	P BIT TEST	X	X
PRP	-1762	PREPARE TO READ	X	X
RCHA	0540	RESET AND LOAD CHANNEL A	X	X
RCHE	-0540	RESET AND LOAD CHANNEL E	X	X
RCHC	0541	RESET AND LOAD CHANNEL C	X	X
RCHD	0541	RESET AND LOAD CHANNEL D	X	X
RCHE	0542	RESET AND LOAD CHANNEL E	X	X
RCHE	0760.00014	RESET CHANNEL TRAPS	X	X
RDCB	0760.01352	RESET DATA CHANNEL B	X	X
RDCB	0760.02352	RESET DATA CHANNEL B	X	X
RDCB	0760.03352	RESET DATA CHANNEL C	X	X
RDCB	0760.04352	RESET DATA CHANNEL D	X	X
RDCB	0760.05352	RESET DATA CHANNEL E	X	X
RDS	0762	READ SELECT	X	X
REW	0772	REWIND	X	X
RQL	-0773	ROTATE MQ LEFT	X	X
RUN	-0772	REWIND AND UNLOAD	X	X
SCMA	0640	STORE CHANNEL A	X	X
SCMB	-0640	STORE CHANNEL B	X	X
SCMC	0641	STORE CHANNEL C	X	X
SCMD	-0641	STORE CHANNEL D	X	X
SCME	0642	STORE CHANNEL E	X	X
SLP	-1762.6BIT14	SENSE SELECT (READ)	X	X
SLW	0602	STORE LOGICAL WORD WITH PARITY	X	X
SSP	0760.00003	SET SIGN PLUS	X	X
STA	0621	STORE ADDRESS	X	X
STD	-0622	STORE DECREMENT	X	X
STO	-0625	STORE INSTRUCTION LOCATION COUNTER	X	X
STO	-0601	STORE	X	X
STO	-0600	STORE MQ	X	X
STR	-1000	STORE LOCATION AND TRAP	X	X
SUP	0502	STORE ZERO	X	X
SWT	0760.0016N	SENSE SWITCH TEST	X	X
TCOA	0600	TRANSFER ON CHANNEL A IN OPERATION	X	X
TCOB	0601	TRANSFER ON CHANNEL B IN OPERATION	X	X
TCOC	0602	TRANSFER ON CHANNEL C IN OPERATION	X	X
TCOD	0603	TRANSFER ON CHANNEL D IN OPERATION	X	X
TCOE	0604	TRANSFER ON CHANNEL E IN OPERATION	X	X
TDOA	-1060	TRANSFER ON CHANNEL A OF FILE IN OP	X	X
TEFA	0030	TRANSFER ON END OF FILE CHANNEL A	X	X
TEFB	-0030	TRANSFER ON END OF FILE CHANNEL B	X	X
TEFC	-0031	TRANSFER ON END OF FILE CHANNEL C	X	X
TEFD	-0031	TRANSFER ON END OF FILE CHANNEL D	X	X
TEFE	-0032	TRANSFER ON END OF FILE CHANNEL E	X	X
TM1	-0120	TRANSFER ON PLUS	X	X
TNZ	-0100	TRANSFER ON NO ZERO	X	X
TOV	0140	TRANSFER ON OVERFLOW	X	X
TRA	0120	TRANSFER ON PLUS	X	X
TRCA	0022	TRANSFER ON REDUNDANCY CHECK CHANNEL A	X	X
TRCB	-0022	TRANSFER ON REDUNDANCY CHECK CHANNEL B	X	X
TRCC	0024	TRANSFER ON REDUNDANCY CHECK CHANNEL C	X	X
TRCD	-0024	TRANSFER ON REDUNDANCY CHECK CHANNEL D	X	X
TRCE	-0026	TRANSFER ON REDUNDANCY CHECK CHANNEL E	X	X
TRP	-1165	TRANSFER AND RESTORE PRIORITY AND TRAPS	X	X
TRT	-1164	TRANSFER AND RESTORE TRAPS	X	X
TSL	-1627	TRANSFER AND STORE INST LOCATION CTR	X	X
TSP	0100	TRANSFER ON ZERO	X	X
VDP	0205	VARIABLE LENGTH DIVIDE OR PROCEED	X	X
VLM	0204	VARIABLE LENGTH MULTIPLY	X	X
WBT	0766.6BIT14	WRITE BLANK TAPE	X	X
WEF	0770	WRITE END OF FILE	X	X
WRS	0766	WRITE SELECT	X	X
XEC	0522	EXECUTE	X	X

DEVICE	CHAN	ADAPT	BCD	BINARY	ADDRESSES
MAGNETIC TAPE	A	0	01201/01212	01221/01232	
	B		02201/02212	02221/02232	
	C		03201/03212	03221/03232	
	D		04201/04212	04221/04232	
	E		05201/05212	05221/05232	
I/O CONTROL UNIT	A		01000	01020	
	B		02000	02020	
	C		03000	03020	
	D		04000	04020	
	E		05000	05020	
DIRECT DATA CONNECTION	B		02240	02260	
	C		03240	03260	
	D		04240	04260	
	E		05240	05260	
1622 CARD READER	A	3	01210	01230	
1622 CARD PUNCH	A	3	01210	01230	
1402 CARD READER	A	3	01211	01231	
1402 CARD PUNCH	A	3	01212	01232	
1453 PAPER WRITER	A	4	01000	01020	
1401 DATA PROC SYSTEM	A	5	01201/01212	01221/01232	
1011 PAPER TAPE READER	A	3	01600	01620	
1009 DATA TRANS UNIT	A	3	01301	01321	
1014 REMOTE INQUIRY UNIT	A	3	01701/01702	01721/01722	
TELEGRAPH TYPE UNITS	A	3	01401/01404	01421/01424	

CPU	PROGRAM	TAPE
CONSOLE	LISTING	UNIT
BCD/BINARY	BCD/BINARY	DIAL
XXX01/XXX21	XXX01/XXX21	1
XXX02/XXX22	XXX02/XXX22	2
XXX03/XXX23	XXX03/XXX23	3
XXX04/XXX24	XXX04/XXX24	4
XXX05/XXX25	XXX05/XXX25	5
XXX06/XXX26	XXX06/XXX26	6
XXX07/XXX27	XXX07/XXX27	7
XXX10/XXX30	XXX0B/XXX28	8
XXX11/XXX31	XXX09/XXX29	9
XXX12/XXX32	XXX10/XXX30	0

NOTES

F - Represents an indirectly addressable instruction
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 N - Represents a number from 1 to 6

EXTENDED PERFORMANCE INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
AXT	0774	ADDRESS TO INDEX TRUE		X
CCS	-341	COMPLEMENT OF ADDRESS IN INDEX		X
LAC	0535	LOAD COMPLEMENT OF ADDRESS IN INDEX		X
LOC	-0535	LOAD COMPLEMENT OF DECREMENT IN INDEX		X
LXA	0534	LOAD INDEX FROM ADDRESS		X
LXD	-0534	LOAD INDEX FROM DECREMENT		X
MIT	-1341.0	STORAGE MINUS TEST		X
MSM	-1623.0	MAKE SIGN MINUS PLUS		X
MSP	-1623.7	STORE SIGN PLUS		X
PAC	0734	PLACE COMPLEMENT OF ADDRESS IN INDEX		X
PAX	0734	PLACE ADDRESS IN INDEX		X
PCS	-1505	PLACE CHARACTER FROM STORAGE		X
PDC	-0737	PLACE COMPLEMENT OF DECREMENT IN INDEX		X
PDX	-0734	PLACE DECREMENT IN INDEX		X
PLT	-1341.7	STORAGE PLUS TEST		X
PT	0734	PLACE INDEX IN ADDRESS		X
PXO	-1754	PLACE INDEX IN DECREMENT		X
SAC	-1623	STORE ACCUMULATOR CHARACTER		X
SXA	0634	STORE INDEX IN ADDRESS		X
SXD	-0634	STORE INDEX IN DECREMENT		X
TIX	2000	TRANSFER ON INDEX		X
TMT	-1704	TRANSMIT		X
TMX	-2000	TRANSFER ON NO INDEX		X
TSX	0074	TRANSFER AND SET INDEX		X
TXH	3000	TRANSFER ON INDEX HIGH		X
TXI	1000	TRANSFER WITH INDEX INCREMENTED		X
TXL	-3000	TRANSFER ON INDEX LOW OR EQUAL		X

7904 DATA CHANNEL DIAGNOSTIC INSTRUCTIONS

INSTRUCTION LISTING-NUMERIC

(All Options)

SYM	NUMERIC	NAME	F	T
LDLB	-0540.1	LOAD DATA REGISTER AND LOOP+CHANNEL B	X	X
LDLC	-0541.1	LOAD DATA REGISTER AND LOOP+CHANNEL C	X	X
LDLD	-0541.1	LOAD DATA REGISTER AND LOOP+CHANNEL D	X	X
LDRE	-0542.1	LOAD DATA REGISTER AND LOOP+CHANNEL E	X	X
SDRC	-0641.1	STORE DATA REGISTER+CHANNEL B	X	X
SDRD	-0641.1	STORE DATA REGISTER+CHANNEL C	X	X
SDRE	-0642.1	STORE DATA REGISTER+CHANNEL D	X	X
SDRE	-0642.1	STORE DATA REGISTER+CHANNEL E	X	X

SINGLE PRECISION FLOATING POINT INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
FAD	0300	FLOATING ADD	X	X
FDP	0241	FLOATING DIVIDE OR PROCEED	X	X
FMP	0260	FLOATING MULTIPLY	X	X
FSB	0302	FLOATING SUBTRACT	X	X
UFM	-0303	UNNORMALIZED FLOATING ADD	X	X
DFM	-0260	UNNORMALIZED FLOATING MULTIPLY	X	X
UFS	-0302	UNNORMALIZED FLOATING SUBTRACT	X	X

DOUBLE PRECISION FLOATING POINT INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
DFAD	0301	DOUBLE PRECISION FLOATING ADD	X	X
DFDP	-0241	DOUBLE PRECISION FLOATING DIVIDE OR PROCEED	X	X
DFMP	0261	DOUBLE PRECISION FLOATING MULTIPLY	X	X
DFSB	0303	DOUBLE PRECISION FLOATING SUBTRACT	X	X

STORAGE PROTECTION INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
RPM	-1004	RELEASE PROTECT MODE		
SPM	-1160	SET PROTECT MODE	X	X

DIRECT DATA CONNECTION INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
PSLB	-0664	PRESENT SENSE LINES+CHANNEL B	X	X
PSLC	-0665	PRESENT SENSE LINES+CHANNEL C	X	X
PSLD	-0665	PRESENT SENSE LINES+CHANNEL D	X	X
PSLE	-0666	PRESENT SENSE LINES+CHANNEL E	X	X
SSLB	-0660	STORE SENSE LINES+CHANNEL B	X	X
SSLC	-0661	STORE SENSE LINES+CHANNEL C	X	X
SSLD	-0661	STORE SENSE LINES+CHANNEL D	X	X
SSLE	-0662	STORE SENSE LINES+CHANNEL E	X	X

1401 OPTION INSTRUCTIONS

SYM	NUMERIC	NAME	F	T
SLFA	-1760.01501	STATUS LINE OFF+CHANNEL A	X	
SLNA	-1760.01541	STATUS LINE ON+CHANNEL A	X	

SYM	NUMERIC	NAME	F	T
TRA	0020	TRANSFER DN REDUNDANCY CHECK+CHANNEL A	X	X
TRCA	0022	TRANSFER DN REDUNDANCY CHECK+CHANNEL B	B	X
TRCC	0024	TRANSFER ON REDUNDANCY CHECK+CHANNEL C	C	X
TRCD	0026	TRANSFER ON REDUNDANCY CHECK+CHANNEL D	D	X
TRCE	0028	TRANSFER ON REDUNDANCY CHECK+CHANNEL E	E	X
TEFA	0030	TRANSFER ON END OF FILE+CHANNEL A	X	X
TEFB	0030	TRANSFER ON END OF FILE+CHANNEL B	X	X
TEFC	0031	TRANSFER ON END OF FILE+CHANNEL C	X	X
TEFD	0031	TRANSFER ON END OF FILE+CHANNEL D	X	X
TEFE	0032	TRANSFER ON END OF FILE+CHANNEL E	X	X
TGAB	0061	TRANSFER ON CHANNEL A IN OPERATION	X	X
TGBC	0062	TRANSFER ON CHANNEL B IN OPERATION	X	X
TGCD	0063	TRANSFER ON CHANNEL D IN OPERATION	X	X
TGCE	0064	TRANSFER ON CHANNEL E IN OPERATION	X	X
TSX	0074	TRANSFER ON ZERO	X	X
TZE	0110	TRANSFER ON NO ZERO	X	X
TNZ	-0100	TRANSFER ON PLUS	X	X
TPL	-0120	TRANSFER ON MINUS	X	X
TMI	-0120	TRANSFER ON OVERFLOW	X	X
TOV	0140	MULTIPLY	X	X
MPY	0200	VARIABLE LENGTH MULTIPLY	X	X
VLM	0204	DIVIDE OR PROCEED	X	X
DVP	0221	VARIABLE LENGTH DIVIDE OR PROCEED	X	X
FDP	0241	FLOATING DIVIDE OR PROCEED	X	X
DFDP	-0241	DOUBLE PREC FLO DIVIDE OR PROCEED	X	X
FMP	0260	FLOATING MULTIPLY	X	X
DFM	0261	DOUBLE PRECISION FLOATING MULTIPLY	X	X
FAD	0300	FLOATING ADD	X	X
UFA	0301	UNNORMALIZED FLOATING ADD	X	X
DFAD	0301	DOUBLE PRECISION FLOATING ADD	X	X
FSB	0302	FLOATING SUBTRACT	X	X
UFS	-0302	UNNORMALIZED FLOATING SUBTRACT	X	X
DFSB	0303	DOUBLE PRECISION FLOATING SUBTRACT	X	X
ANA	0340	COMPARE ACCUMULATOR WITH STORAGE	X	X
CAS	0340	LOGICAL COMPARE ACCUM WITH STORAGE	X	X
LUR	0340	ADD AND CARRY LOGICAL WORD	X	X
ACL	0361	ADD	X	X
ADD	0400	SUBTRACT	X	X
SUB	0402	HALT AND PROCEED	X	X
HPR	0420	CLEAR AND ADD	X	X
CLA	0500	CLEAR AND ADD LOGICAL WORD	X	X
CLA	-0500	OR TO ACCUMULATOR	X	X
ORA	0501	CLEAR AND SUBTRACT	X	X
CLS	0502	EXECUTE	X	X
XEC	0522	LOAD INDEX FROM ADDRESS	X	X
LXA	0534	LOAD INDEX FROM DECREMENT	X	X
LXD	-0534	LOAD COMPLEMENT OF ADDRESS IN INDEX	X	X
LAC	0535	LOAD COMPLEMENT OF DECREMENT IN INDEX	X	X
LIC	-0535	RESET AND LOAD CHANNEL A	X	X
RCHA	0540	RESET AND LOAD CHANNEL B	X	X
RCHB	0540	RESET AND LOAD CHANNEL C	X	X
RCHD	0540.1	RESET AND LOAD CHANNEL D	X	X
RCHE	0541	RESET AND LOAD CHANNEL E	X	X
LDB	0541	LOAD DATA REGISTER AND LOOP+CHANNEL B	X	X
RCDA	0541	LOAD DATA REGISTER AND LOOP+CHANNEL C	X	X
LDLC	0541.1	LOAD DATA REGISTER AND LOOP+CHANNEL D	X	X
RCDE	0542	RESET AND LOAD CHANNEL D	X	X
LDL	0542.1	LOAD DATA REGISTER AND LOOP+CHANNEL E	X	X
LDQ	0560	LOAD MQ	X	X
ENB	0564	ENABLE FROM Y	X	X
STZ	0565	STORE ZERO	X	X
STQ	0566	STORE MQ	X	X
STO	0601	STORE	X	X
SLW	0602	STORE LOGICAL WORD	X	X
STA	0621	STORE ADDRESS	X	X
STD	0622	STORE DECREMENT	X	X
STL	-0625	STORE INSTRUCTION LOCATION COUNTER	X	X
SXA	0634	STORE INDEX IN ADDRESS	X	X
SXA	-0634	STORE CHANNEL A	X	X
SCHA	0640	STORE CHANNEL B	X	X
SCHB	-0640	STORE DATA REGISTER+CHANNEL B	X	X
SDRB	-0640.1	STORE CHANNEL C	X	X
SCHC	0641	STORE CHANNEL C	X	X
SDRC	0641.1	STORE CHANNEL D	X	X
SCHD	-0641	STORE REGISTER+CHANNEL C	X	X
SDRD	-0641.1	STORE CHANNEL D	X	X
SCHE	0642	STORE CHANNEL E	X	X

INSTRUCTION LISTING-NUMERIC

LOGIC FLOW

(All Options)

SYM	NUMERIC	NAME	F	T
SDRE	0642, I	STORE DATA REGISTER, CHANNEL E	X	X
SSLB	0660	STORE SENSE LINES, CHANNEL B	X	X
SSLC	0661	STORE SENSE LINES, CHANNEL C	X	X
SSLD	0661	STORE SENSE LINES, CHANNEL D	X	X
SSLE	0662	STORE SENSE LINES, CHANNEL E	X	X
PSLB	0664	PRESENT SENSE LINE, CHANNEL B	X	X
PSLC	0665	PRESENT SENSE LINES, CHANNEL C	X	X
PSLD	0665	PRESENT SENSE LINES, CHANNEL D	X	X
PSLE	0666	PRESENT SENSE LINES, CHANNEL E	X	X
PAX	0734	PLACE ADDRESS IN INDEX		
PDX	0734	PLACE DECREMENT IN INDEX		
PAC	0737	PLACE COMPLEMENT OF ADDRESS IN INDEX		
PDC	0737	PLACE COMPLEMENT OF DECREMENT IN INDEX		
PX	0734	PLACE INDEX IN ADDRESS		
PXD	0734	PLACE INDEX IN DECREMENT		
LBT	0760, 000001	LOW ORDER BIT TEST	X	
PBT	0760, 000001	P BIT TEST	X	
CHS	0760, 000002	CHANGE SIGN	X	X
SSP	0760, 000003	SET SIGN PLUS	X	X
ENK	0760, 000004	ENTER KEYS	X	X
IO	0760, 000005	INPUT/OUTPUT CHECK TEST		
COM	0760, 000006	COMPLEMENT MAGNITUDE	X	X
DCT	0760, 000112	DIVIDE CHECK TEST	X	X
RCT	0760, 000114	RESTORE CHANNEL TRAPS	X	X
SWT	0760, 001616	SENSE SWITCH TEST	X	X
ETTA	0760, 010009	END OF TAPE TEST, CHANNEL A	X	X
RDTA	0760, 013522	RESET DATA CHANNEL A	X	X
ETTB	0760, 020009	END OF TAPE TEST, CHANNEL B	X	X
RDTB	0760, 023522	RESET DATA CHANNEL B	X	X
ETTC	0760, 030009	END OF TAPE TEST, CHANNEL C	X	X
RDCC	0760, 033522	RESET DATA CHANNEL C	X	X
ETTD	0760, 040009	END OF TAPE TEST, CHANNEL D	X	X
RDCD	0760, 043522	RESET DATA CHANNEL D	X	X
RDC	0760, 050009	END OF TAPE TEST, CHANNEL E	X	X
RDCE	0760, 053522	RESET DATA CHANNEL E	X	X
RDS	0762	READ SELECT	X	X
LLS	0763	LONG LEFT SHIFT	X	X
LGL	0763	LOGICAL LEFT SHIFT	X	X
BSR	0764	BACKSPACE RECORD	X	X
LGR	0765	LONG RIGHT SHIFT	X	X
GLR	0765	LOGICAL RIGHT SHIFT	X	X
WBT	0766, 6BIT14	WRITE BLOCK TAPE	X	X
WRS	0766	WRITE SELECT	X	X
ALS	0767	ACCUMULATOR LEFT SHIFT	X	X
WER	0770	WRITE END OF FILE	X	X
ARS	0771	ACCUMULATOR RIGHT SHIFT	X	X
DRW	0772	REWIND	X	X
RUN	0772	READ AND UNLOAD	X	X
RQD	0773	ROTATE MQ LEFT	X	X
AXT	0774	ADDRESS TO INDEX TRUE	X	
STR	1-000	STORE LOCATION AND TRAP		
TXI	1-000	TRANSFER WITH INDEX INCREMENTED		
RPI	1-004	RELEASE PROTECT MODE		
TDOA	1-160	TRANSFER ON CHANNEL A DEVICE IN OP	X	X
SPM	1-160	SET PROTECT MODE	X	X
TRT	1-164	TRANSFER AND RESTORE TRAPS	X	X
TRD	1-165	TRANSFER AND RESTORE PARITY AND TRAPS	X	X
VMA	1-204	VARIABLE LENGTH MULTIPLY AND ACCUM	X	X
CCS	1-341	COMPARE CHARACTER WITH STORAGE	X	X
MS	1-341, 6	STORAGE MINUS TEST	X	X
PLT	1-341, 7	STORAGE PLUS TEST	X	X
PCS	1-505	PLACE CHARACTER FROM STORAGE	X	X
CAP	1-510	CLEAR AND ADD LOGICAL WORDS WITH PARITY	X	X
SLP	1-612	STORE LOGICAL WORD WITH PARITY	X	X
SAC	1-623	STORE ACCUMULATOR CHARACTER	X	X
MSM	1-623, 6	MAKE STORAGE SIGN MINUS	X	X
MSP	1-623, 7	MAKE STORAGE SIGN PLUS	X	X
TTR	1-704	TRANSFER AND STORE INSTR LOCATION COUNTER	X	X
ICT	1-760, 000114	INHIBIT CHANNEL TRAPS	X	X
SFLA	1-760, 0150	STATUS LINE OFF, CHANNEL A	X	X
SLNA	1-760, 0154	STATUS LINE ON, CHANNEL A	X	X
PRO	1-762	PREPARE TO READ	X	X
SEN	1-762, 6BIT14	SENSE SELECT XREAD	X	X
CTR	1-762, 6BIT14	COMPARE SELECT XWRITE	X	X
PWR	1-764	PREPARE TO WRITE	X	X
TIX	2-000	TRANSFER ON NO INDEX		
TXN	2-000	TRANSFER ON INDEX HIGH		
TXH	3-000	TRANSFER ON INDEX HIGH		
TXL	3-000	TRANSFER ON INDEX LOW OR EQUAL		

NOTES

F — Represents an indirectly addressable instruction
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Inst	Action	Result/ Registers
ACL	C(AC)P, 1-35 + C(Y) C(AC), Q are unchanged	AC
ADD	C(AC) + C(Y)	AC
ALS	← C(AC)Q, P, 1-35	AC
ANA	C(AC)P, 1-35 AND'ed with C(Y) C(AC), Q are set to zeros	AC
ARS	C(AC)Q, P, 1-35 →	AC
AXT	C(AXT)21-35 replace C(XR)	Index
CAL	C(AC)P, 1-35 replaced by C(Y)	AC
CAP	C(AC)S, Q are set to zeros C(AC)S, P, 1-35 are replaced by C(Y)C, S, 1-35 C(AC)Q is set to zero	AC
CAS	If C(AC) > C(Y) C(AC) = C(Y) C(AC) < C(Y)	Next Inst 2nd Inst 3rd Inst
CHS	C(AC)S is inverted	AC
CLA	C(AC)Q, P, 1-35 are unchanged C(AC)S, 1-35 are replaced by C(Y)	AC
CLS	C(AC)Q, P are set to zeros C(AC)S, 1-35 are replaced by negative of C(Y) C(AC)Q, P are set to zeros	AC
COM	C(AC)Q, P, 1-35 are replaced by negative of itself C(AC)S is unchanged	AC
DVP	C(AC)Q, P, 1-35 & C(MQ)1-35 + C(Y)	AC (remainder) MQ (quotient)
LAC	2's comp of C(Y)21-35 replace C(XR)	Index
LAS	If C(AC)Q, P, 1-35 > C(Y) C(AC)Q, P, 1-35 = C(Y) C(AC)Q, P, 1-35 < C(Y)	Next Inst 2nd Inst 3rd Inst
LDC	2's comp of C(Y)3-17 replace C(XR)	Index
LDQ	C(MQ) replaced by C(Y)	MQ
LGL	← C(AC)Q, P, 1-35 & C(MQ)S, 1-35	AC & MQ
LGR	C(AC)Q, P, 1-35 & C(MQ)S, 1-35 →	AC & MQ
LLS	← C(AC)Q, P, 1-35 & C(MQ)1-35	AC & MQ
LRS	C(AC)Q, P, 1-35 & C(MQ)1-35 →	AC & MQ
LXA	C(Y)21-35 replace C(XR)	Index
LXD	C(Y)3-17 replace C(XR)	Index
MPY	C(Y) * C(MQ)	AC (low order) MQ (high order)
ORA	C(AC)P, 1-35 OR'ed with C(Y)	AC
PAC	2's comp of C(AC)21-35 replace C(XR)	Index
PAX	C(AC)21-35 replace C(XR)	Index
PDC	2's comp of C(AC)3-17 replace C(XR)	Index
PDX	C(AC)3-17 replace C(XR)	Index
PXA	C(XR) replace C(AC)21-35	AC
PXD	C(AC)S, 1-20 are set to zeros C(XR) replace C(AC)3-17	AC
RQL	← C(MQ)S, 1-35	MQ
STA	C(Y)21-35 replaced by C(AC)21-35	Loc Y
STD	C(Y)S, 1-20 are unchanged C(Y)3-17 replaced by C(AC)3-17 C(Y)S, 1, 2, 18-35 are unchanged	Loc Y
STO	C(AC)S, 1-35 replace C(Y)	Loc Y
STQ	C(MQ)S, 1-35 replace C(Y)	Loc Y
STZ	Zeros replace C(Y)	Loc Y
SUB	C(AC) - C(Y)	AC
SXA	C(XR) replace C(Y)21-35	Loc Y
SXD	C(Y)S, 1-20 are unchanged C(XR) replace C(Y)3-17 C(Y)S, 1, 2, 18-35 are unchanged	Loc Y

Read Bus Position	Rd Bus B	Rd Bus A	Rd Bus 8	Rd Bus 4	Rd Bus 2	Rd Bus 1
1st Word Spec by RCHA	Position Sign	Position 1	Position 2	Position 3	Position 4	Position 5
MACHINE AND OP	NOT READY		CHECK	BUSY	CONDITION	NO TRANSFER
1401 DPS	1401 Busy	Not Used	Not Used	Not Used	Not Used	Not Used
1402 Card Read Operation	Out of Cards; no End of File. Off line. Reader power off, Stop key depressed.		Card codes other than 64 valid char. Check status not turned off with SENA instruction. Chan A redundancy chk turned on when card RDS is given. Hole count, parity, ring check, or clock error.	Card filling the buffer.	Status bit indicates EOF and is turned on after the last card has been transferred from buffer to CPU if EOF key has been depressed. Indicator sensed and turned off by SENA instruction, if reader is not busy.	Used with column binary feature on 1414-4 and indicates the card in the read buffer had 7 and 9 punches in column one, and there are 160 characters of information available.
1402 Card Punch Operation	Out of cards. Off line. Power off. Stop key depressed.		Not Used	Punching a card.	Hole count check on 1st card while 2nd is being punched, clock ring or parity error in punch scans.	Not Used
1403 Printer Operation	Out of forms. Off line. Power off. Stop key depressed.	Forms Busy	Same as conditions given in Position 4.	Printer printing a line or forms busy.	Parity error detected during a print scan. A print hammer failed to fire. Printer timing circuit was out of sync with print chain.	Not Used
1009 Data Transmission Unit (Input Status)	Off line. Power off.		A parity error was detected during filling of the buffer.	Buffer being filled.	CPU did not empty the buffer in time and a message has been lost.	End of message, or no message is in the buffer.
1009 Data Transmission Unit (Output Status)	Off line. Power off.		Not Used	Both buffers have data, one is emptying.	Last message sent had an error. Message was transmitted to the local 1009 but was not sent successfully to the remote 1009.	End of message.

1011 Paper Tape Reader	Out of tape. Tape broken. Off line. Power off.		Parity error while buffer was being loaded.	Buffer being filled.	Not Used	Not Used
1014 Remote Inquiry Unit (Input Status)	Off line. Power off.		Error was detected during filling of the buffer.	Not Used	Not Used	No message in the buffer. Buffer being filled.
1014 Remote Inquiry Unit (Output Status)	Off line. Power off.		Not Used	Buffer being emptied.	Error was detected during sending of previous message.	Previous message was not sent; station addressed inoperative.
Teletypewriter Type Input-Output (Input Status)	Buffer off line. Power off.		Parity error during filling of buffer. Format chk during filling of buffer. Part of a message has been lost.	Buffer being filled.	CPU did not empty buffer in time and one or more messages have been lost.	No message in the buffer.
Teletypewriter Type Input-Output (Output Status)	Buffer off line. Power off. Local teletypewriter unit is not ready.		Not Used	Buffer being emptied.	An error was detected during the transmission of the previous message.	Previous message was sent but received incorrectly or not at all, because of invalid format, line failure, or excessive delay in getting characters to the output line.
Tapes	Ready	Not Used	Not Used	Sense Rewind	Not Used	Sense Load Point

Normal Sequence:

SENA - 1762

RCHA + 0540

5	1	11	12	13	14	15
1	0	1	1	1	0	0
0	0	0	1	0	0	0

MASKING FOR DIRECT DATA AND CHANNEL TRAPS

Mask Trigger	Conditions Enabled and Tags Stored	Channel	Mask Tgr Set by ENB Data Wr Bit
Operation	Operation Complete 17 End of File 15 and 17	A B	35 34
	Word Parity 14 and 17 Unusual End 12 and 17	C D E	33 32 31
Direct Data	Direct Data Interrupt 16 (B) 15 (C) 14 (D) 13 (E)	B C D E	25 24 23 22
	Word Parity 14 Redundancy Check 16	A B C D E	17 16 15 14 13
Attention	1401 Attention Tele-Processing Interrupt (1414 Attention) 10 SI Attention 11	A B C D E	8 7 6 5 4
	Unit Record	Unit Record Interrupt	8 A S

TRAP-CONTROL SET AND RESET

	Trap Control (02.13.03)	Parity Mode (02.13.03)	Channel Trap Ct (02.13.03)	MP Mode (02.16.05)
Set	1. TRT or TRP Inst 2. Power on Reset 3. Reset, Load, or Clear Keys	1. TRP Inst 2. Power on Reset 3. Reset, Load, or Clear Keys	1. ENB or RCT Inst	1. SPM Inst
Reset	1. Any Trap	1. Parity Trap	1. Channel or DD Trap 2. ICT Inst 3. Power on Reset 4. Reset, Load or Clear Keys	1. SPM, RPM MP Violation, or Pre I-O Traps 2. Power on Reset 3. Reset, Load, or Clear Keys

TRAPPING

TRAP PRIORITY	TRAP NAME	REASON FOR TRAP	WHEN TRAP CAN OCCUR	TRAP RESTRICTIONS	STORE *8 LOCATION	TRANSFER *9 LOCATION	DISABLING EFFECT OF TRAP	HOW DISABLING EFFECT MAY BE NULLIFIED	MATERIAL OF TRAPPING
1	Interval Timer Blast	A "C" cycle request is received before the preceding "C" cycle request is honored. 33 milliseconds have expired since the interval timer was last stepped.	A "C" cycle request may occur (and therefore a Trap request) 1) Between instructions 2) During RDS, PRD, SEN, WRS, PWR, CTR, BSR, REW, WBT, RUN, WEF instructions. 3) Between "U" cycles during execution of a RCHA instruction. A trap request initiates an immediate trap.	None	00036	00037	1) Trap control turned off 2) Resets all channels 3) Resets program reg. in CPU and shift ctr. 4) Resets waiting "C" cycle requests and interval timer overflow trap requests. 5) Interval timer will contain z_2 less than it should. 6) An interrupted instruction is not completed.	Trap control may be turned on by executing a TRT or TRP instruction. Interval timer may be corrected by: CLA 0005 ADD =02 STO 0005	
2 **	Memory Protect Violation	A store is attempted in a protected area of core. NOTE: Input information from an I/O device is never prevented from storing in a protected area.	Immediately after an "E" cycle attempting (it will not succeed) to store in a protected area of core.	1) Trap control on *! 2) Protect mode on *! If trap control is off, protect mode on, and a violation occurs, the store will be successful and a trap will not occur.	00032 Bit 16 Flag	00033	1) Protect mode turned off. 2) Violating instructions are not allowed to store (or complete, in the case of the Transmit Instruction; on other instructions, the E store cycle will be the last cycle.) 3) Trap control turned off.	Protect mode may be turned on by executing a SPM instruction. Trap control may be turned off by executing a TRT or TRP instruction.	

TRAP PRIORITY	TRAP NAME	REASON FOR TRAP	WHEN TRAP CAN OCCUR	TRAP RESTRICTIONS	STORE *8 LOCATION	TRANSFER *9 LOCATION	DISABLING EFFECT OF TRAP	HOW DISABLING EFFECT MAY BE NULLIFIED
3 ** MP Violation and Parity traps have no priority over each other, because when one of the errors occurs, the other is not possible in the same instruction.	Parity	Storage parity error during: 1) "I" or "IA" cycles 2) "E" or "C" cycles which do not store. NOTE: Parity is not checked during the "E" cycle of a CAP instruction. "B" or "U" Cycle parity errors will not cause a parity trap. A channel trap may be requested if the operation or parity mask bit is enabled for that channel. See channel traps. If bad parity is detected when <u>reading</u> out of core during any type cycle, the word is regenerated back in core with bad parity.	1) Immediately after the "I", "IA", or "E" cycle causing the parity error. An instruction requiring additional cycles will not complete. 2) For a parity error during a "C" cycle taken during the execution of an instruction, the instruction will be allowed to complete before the trap is initiated. 3) For a parity error during a "C" cycle taken between instructions, the trap will be immediate.	1) Trap control on *2 2) Parity control on *2 *2 parity errors detected with either trap control or parity off do not cause an immediate trap and do not interrupt an instruction. However, the error is remembered and will cause a trap as soon as trap and parity control are on.	00040 Bit S Flag indicates error occurred when parity or trap control was off. *2 Bit 1 Flag "C" cycle error. Bit 18 Flag "I" or "IA" cycle error. Bit 19 Flag "E" cycle error. Bits 3-17 will contain the location in error if not a "C" cycle or delayed error.	00041	1) Trap control turned off. 2) Parity control turned off. 3) Parity errors detected during multi-cycle instructions will prevent any remaining cycles from being taken to complete the instruction.	Trap control and parity control may be turned on by executing a TRP instruction. Trap control may be turned on and parity control left off by executing a TRT instruction.

4 All instruction traps are mutually exclusive and therefore have no priority with regard to each other. *7 If a parity error occurs during an I or IA cycle for this instruction, a parity trap occurs and the instruction trap does not occur. The IA cycle of a violating SPM instruction, however, cannot cause a parity trap.	SPM*7	SPM instruction with protect mode on.	Execution of SPM instruction causes the trap.	Protect mode on	00032 Bit 16 Flag	00033	1) Protect mode turned off. 2) Trap control turned off.	Protect mode may be turned on by executing another SPM instruction. See Note below.
	RPM*7	RPM instruction	Execution of RPM instruction causes the trap.	None	00032 Protect mode On Off Bit 15 Bit 14 Flag Flag	00033	1) Protect mode turned off. 2) Trap control turned off.	Protect mode may be turned on by executing a SPM instruction. See Note below.
	STR*7	STR instruction.	Execution of STR instruction causes the trap.	None	00000	00002	Trap control turned off	See Note below.
	Floating Point	Floating-point instruction and any one or combination of the following: 1) AC char. computed to exceed 377. 2) MQ char. computed lower than 000 3) AC char. computed lower than 000*3 4) MQ char. computed to exceed 377*4 5) High order double precision operand address ODD. 6) Doubles precision instruction executed on machine with single precision only. *3 can occur without (2) during divide only. *4 can occur without (1) during divide only.	After completion of instruction for (1) + (2) + (3) + (4). After first "E" cycle for (5) instruction will not complete. After first I cycle for (6); instruction will not complete.	None	00000 (5) yields Bit 12 Flag (1) + (4) yields Bit 15 Flag (1) + (3) yields Bit 16 Flag (2) + (4) yields Bit 17 Flag (1) + (2) + (3) + (4) during single prec. Divide yields Bit 14 Flag (6) yields sign bit	00010	1) Instruction not completed for (5) and (6). 2) Trap control turned off.	See Note below. Note: Trap control may be turned on by executing a TRT or TRP instruction.

TRAP PRIORITY	TRAP NAME	REASON FOR TRAP	WHEN TRAP CAN OCCUR	TRAP RESTRICTIONS	STORE *8 LOCATION	TRANSFER *9 LOCATION	DISABLING EFFECT OF TRAP	HOW DISABLING EFFECT MAY BE NULLIFIED
5	Pre-Interrupt Memory Protect	Interval timer overflow, channel or direct data trap requested with protect mode on.	Trap is initiated at the time the causitive trap would have been initiated had memory protect been off. Refer to individual causitive trap descriptions.	1) Trap control on. 2) Protect mode on. 3) Restrictions for causitive trap met.	00032 Bit 17 Flag	00033	1) Protect mode turned off. 2) Delays execution of causitive trap until protect mode is turned off. 3) Trap control turned off.	1) Protect mode may be turned on by executing a SPM instruction. 2) Trap control may be turned on by executing a TRT or TRP instruction.
6	Interval Timer Overflow	Adder 1 carry while interval timer is being incremented.	After "C" cycle storing - incremented interval timer if "C" cycle occurred between instructions. If "C" cycle occurred during a BSR, REW, RUN, WEF or RCHA instruction, the instruction will complete before trap is initiated. If the trap request occurs during or immediately after a privileged *5 instruction, the trap will be delayed until after the completion of the instruction following the privileged instruction.	1) Trap control on. 2) Protect mode off. *6 *6 If on, pre-interrupt memory protect trap will be initiated to turn if off.	00006	00007	1) Blocks "C" cycle requests while waiting for trap to be executed. 2) Trap control turned off. Trap control may be restored by executing a TRT or TRP instruction.	If trap execution is delayed long enough to block two "C" cycle requests, an interval timer blast trap will be initiated which will reset overflow trap request. At this time, the interval timer should contain z_2 (it will contain 0g). This may be corrected by: CL A =02 STO 00005

7	Direct Data	Interrupt signal from direct data external device with direct data mask bit for subject channel a one.	After completion of the instruction in progress when the interrupt signal is received. If the trap request occurs during or immediately after a privileged *5 instruction, the trap will be delayed until after the completion of the instruction following the privileged instruction.	1) Trap control on. 2) Channel trap control on. 3) Protect mode off. *10 4) Direct data mask bit for interrupting channel must be a one *11.	00003 Channel B interrupt yields Bit 16 Flag Channel C interrupt yields Bit 15 Flag Channel D interrupt yields Bit 14 Flag Channel E interrupt yields Bit 13 Flag	00004 The instruction contained in this location must be an unconditional transfer to maintain 7090/94 compatibility.	control turned off. Channel trap control may also be turned off by executing an RCT instruction. Direct data traps may also be blocked by an ENB O instruction.	control may be turned on by executing a RCT or ENB instruction. The RCT instruction will allow the mask bits specified in the last ENB instruction to retain control. Any interrupt signal received while channel trap control was off will be honored after execution of RCT along with TRT or TRP. The ENB instruction will permit an interrupt signal received while channel trap control was off to cause a trap if the mask bit for the channel is turned on by the new ENB instruction, even
				*10 If on, pre-interrupt memory protect trap will be initiated to turn if off.	*11 Flag Bits will be stored only if the mask bit is on. It is possible to have more than one Flag Bit stored if the execution of the trap is delayed long enough to allow more than one channel to send an interrupt signal. Only one trap will be executed in this case.			

TRAP PRIORITY	TRAP NAME	REASON FOR TRAP	WHEN TRAP CAN OCCUR	TRAP RESTRICTIONS	STORE *8 LOCATION	TRANSFER *9 LOCATION	DISABLING EFFECT OF TRAP	HOW DISABLING EFFECT MAY BE NULLIFIED
								though the prior ENB instruction did not specify that mask bit.
8 Trap priority among channels is in order of	Channel E Channel D Channel C	1) An I/O operation completes with operation "mask bit for subject channel a one. This will occur whenever any channel	After completion of the instruction in progress when the trap request is generated. A trap request may be generated by a channel only when it goes not in	1) Trap control on 2) Channel trap control on 3) Protect mode off *12	00022 *15 00020 *15 00016 *15	00023 *14 00021 *14 00017 *14	1) Channel trap control turned off. Channel trap control may also be turned off by executing an ICT instruction.	Waiting interrupt requests are reset by a direct data trap (only for those channels covered by a mask bit) an RDCX instruction(all channels) or by reading or writing from the DD channel requesting the interrupt. 1) Channel trap control may be turned on by executing a RCT or ENB instruction. 2) Trap control may be turned on by executing a TRT or TRP instruction.

physical remoteness from CPU. Channel "A" has the lowest priority. For this discussion, it is assumed that Channel "P" is the furthest from CPU. No channel may request a trap (except an attention trap) while it is still in use. However, the condition that will eventually cause a trap request may be present for much of the channel operation. If a higher priority	Channel B Channel A	command completes, tapes complete a back space or write end of file or blank tape, or when the relays pick for a rewind. 2) Redundancy check from I/O device or channel parity error with "parity" mask bit for subject channel a one *18. This will stop the transmission of data although the channel will remain in use. 3) End of file *13,18 from tapes or from 1401 (KB instruction from 1401), or when 1622 or 1402 reader runs out of cards with "operation" mask bit a one. 4) Word parity error while reading or writing from core during "U" or "B" cycles or channel parity error during a write operation. Either "parity" mask bit (data transmission stops) or "operation" mask bit	use. The exception to this is an attention request which does not have to wait until the channel goes not in use. If the trap request occurs during or immediately after a privileged*5 instruction, the trap will be delayed until after the completion of the instruction following the privileged instruction.	4) Appropriate mask bit must be on for both the channel and the condition for which the trap is requested. *12 If on, pre-interrupt memory protect trap will be initiated to turn it off.	00014 *15 00012 *15	00010 00013 *14 *14	Channel traps may also be blocked by an ENB O instruction. This is not advisable however because data transmission will not be stopped in the event of a parity error or redundancy check with the "parity" mask bit off. This will also make it difficult to locate the word in error because the channel address counter will continue to step after the error occurs. 2) Trap control turned off.	mask bits specified in the last ENB instruction to retain control. Any trap request received while channel trap control was off will be honored after execution of RCT along with TRT or TRP. The ENB instruction will permit a trap request occurring while channel trap control was off to be honored if the mask bit for both the channel and the condition is turned on by the new ENB instruction, even though the prior ENB instruction did not specify that mask bit.
					*15 (1) yields bit 17 Flag (2) yields bit 16 flag (3) yields bits 15 and 17 flag (4) yields bit 14 flag (5) yields bits 12 and 17 flag (6) yields bit 11 flag (7) yields bit 10 flag (8) yields bit 9 flag			

TRAP PRIORITY	TRAP NAME	REASON FOR TRAP	WHEN TRAP CAN OCCUR	TRAP RESTRICTIONS	STORE *8 LOCATION	TRANSFER *9 LOCATION	DISABLING EFFECT OF TRAP	HOW DISABLING EFFECT MAY BE NULLIFIED
channel goes "not in use" and requests a trap, it will trap first, even though the condition that caused its trap occurred after a trapping condition in the channel that is still in use.		(transmission continues) must be a one. 5) Unusual end signal from simplex interface I/O device *16, or tape word incomplete (number of characters sent to tape, or received from tape, except tape mark, not a multiple of six). Operation mask bit must be a one. The significance of the simplex interface signal depends upon the simplex interface device and it will usually require a sense operation to determine the condition. 6) Simplex interface *16 attention signal with "attention" mask bit a one. The significance of the signal depends upon the simplex interface I/O device. 7) 1401 attention signal *17 with "attention" mask bit a one. The attention			(9) yields bit 8 flag More than one bit may be stored if the trap execution is delayed long enough to allow multiple trapping conditions to occur on a single channel. Only the first condition will request a trap.			The conditions that will request a trap can be reset by executing the trap for that channel or by a RDCX instruction (this will reset <u>all</u> trapping conditions on the specified channel).

SUMMARY OF MASK BITS FOR CHANNEL AND DIRECT DATA TRAPS					
Channel	Bit Position of ENB Operand				
	Operation	Parity	Attention	Unit Record	Direct Data
E	31	13	4	N/A	22
D	32	14	5	N/A	23
C	33	15	6	N/A	24
B	34	16	7	N/A	25
A	35	17	8	S	N/A

*5 Privileged instructions are: RDS, PRD, SEN, WRS, PWR, WBT, CTR, ENB, RCT, ICT, XEC, SPM

*6 The core address of the instruction following the instruction being executed when a trap request occurs will be stored in positions 21-35 of the store location, in addition to any indicated flag bits.

*7 The final operation during a trap consists of starting memory with this address selected during I time.

*8 Channel "A" end of file cannot directly cause a trap, but will induce an "operation" complete "Trap." In this case bits will be stored in positions 15 and 17 of Location 00012.

*9 Overlap channels only for simplex interface unusual end signal.

*10 Channel "A" only

*11 If the mast bit for redundancy check or end of file is a one, the respective TRCX or TEFX instructions will always be executed as no-operations regardless of whether the tested conditions exist.

LOGIC PAGE LOCATIONS

Caution

When scoping, avoid ground levels such as minus B and plus S. A ground level could be an open circuit.

Caution

Do not use an ungrounded scope

LIGHT LOCATIONS

The location of indicator lights is noted in the following charts by--

- C Console
- N No indicator light
- P Back panel mounting

7040/44 CPU

MFI CODES

AT INTERVAL TIMER
 CH8 FIRST OVERLAP CHANNEL - CHANNEL B
 CHC ADDITIONAL OVERLAP CHANNEL - CHANNEL C
 CHO ADDITIONAL OVERLAP CHANNEL - CHANNEL D
 CHE ADDITIONAL OVERLAP CHANNEL - CHANNEL E
 EP EXTENDED PERFORMANCE
 SP SINGLE PRECISION FLOATING POINT
 DP DOUBLE PRECISION FLOATING POINT
 MP MEMORY PROTECT 4K
 MPB MEMORY PROTECT 8K
 MP16 MEMORY PROTECT 16K
 MP32 MEMORY PROTECT 32K
 BU 8 USEC MEMORY
 2.5U 2.5 USEC MEMORY
 4K 4K MEMORY
 4KBK 4K OR 8K MEMORY
 16K 16K MEMORY

KEYS AND SWITCHES

NAME	ALD PAGE FROM	ALD PAGE TO	VOL
ADDRESS - OPK 21 TO 35-	N 00.20.04.0	02.05.21.1	V3
AK 21 TO 35 -LOCATION	N 00.20.04.0	02.04.21.1	V3
ANY KEY -RESET-	N 00.20.06.0	02.14.01.1	V4
AUTOMATIC	C 00.20.06.0	02.14.06.1	V4
CHANNEL 8BIT DENSITY -ABCOE-	N 00.20.00.0	02.04.04.1	V3
CHANNEL DENSITY -ABCDE-	N 00.20.00.0	02.04.04.1	V3
C-B AND THERMAL LIGHT	C 09.00.50.0		V7
CLEAR	N 00.20.06.0	02.14.04.1	V4
CONTINUOUS FNTTR INSTRUCTION	C 00.20.06.0	02.14.06.1	V4
DISPLAY STORAGE	N 00.20.06.0	02.14.03.1	V4
EMERGENCY OFF PULL	N 09.00.10.0	SHEET.1	V7
EMERGENCY POWER OFF	N 09.00.10.0	SHEET.1	V7
ENTER INSTRUCTION	N 00.20.06.0	02.14.03.1	V4
ENTER STORAGE	N 00.20.06.0	02.14.03.1	V4
I-O INTERLOCK CONTROL	C 00.20.06.0	02.14.06.1	V4
I-O INTERLOCK -CONTROL-	C 00.20.06.0	02.14.06.1	V4
INSTRUCTION -OPK 0 TO 17-	N 00.20.04.0	02.05.00.1	V3
LOAD	N 00.20.06.0	02.14.04.1	V4
LOCATION -AK 21 TO 35	N 00.20.04.0	02.04.21.1	V3
MASTER CONNECT LIGHT	C 09.00.50.0		V7
MASTER CONNECT	C 09.00.10.0	SHEET.1	V7
MASTER DISCONNECT	C 09.00.10.0	SHEET.1	V7
MASTER POWER CONNECT LIGHT	C 09.00.50.0		V7
MASTER POWER CONNECT	C 09.00.10.0	SHEET.1	V7
MASTER POWER DISCONNECT	C 09.00.10.0	SHEET.1	V7
MULTIPLE STEP	N 00.20.06.0	02.14.01.1	V4
NORMAL POWER OFF	N 09.00.30.0	SHEET.1	V7
NORMAL POWER ON	N 09.00.30.0	SHEET.1	V7
NORMAL POWER ON LIGHT	C 09.00.50.0		V7
OPK 18 TO 20 -TAG-	N 00.20.04.0	02.05.18.1	V3

NAME	ALD PAGE FROM	ALD PAGE TO	VOL
21 TO 35 -ADDRESS	N 00.20.04.0	02.05.21.1	V3
0 TO 17 -INSTRUCTION	N 00.20.04.0	02.05.00.1	V3
OVER OFF -NORMAL-	N 09.00.30.0	SHEET.1	V7
POWER ON -NORMAL-	N 09.00.30.0	SHEET.1	V7
POWER ON LIGHT -NORMAL-	C 09.00.50.0		V7
RESET	N 00.20.06.0	02.14.04.1	V4
RESET - ANY KEY-	N 00.20.06.0	02.14.01.1	V4
ENSE -123456-	N 00.20.04.1	02.10.75.1	V4
ENSE SWITCHES -123456-	N 00.20.04.1	02.10.75.1	V4
INGLE STEP	N 00.20.06.0	02.14.01.1	V4
TART	N 00.20.00.1	02.14.02.1	V4
TER MODE	N 00.20.00.1	02.14.02.1	V4
TER MODE CYCLE	N 00.20.00.1	02.14.03.1	V4
TORAGE CLOCK	N 00.20.04.0	02.05.18.1	V3
AG - OPK 18 TO 20-			

REGISTERS

NAME	ALD PAGE	VOL	MFI
ACCUMULATOR	C 02.02.00.1	V2	
ADDRESS REGISTER	C 02.04.21.1		
CLOCK	C 02.15.00.1	V4	
COUNT REGISTER 32-35	N 02.16.01.1	V4	MP
FIELD REGISTER 21-27	N 02.16.02.1	V4	MP
INOEX REGISTER	C 02.03.21.1	V3	
INSTRUCTION COUNTER	C 02.04.21.1		
INSTRUCTION REG. S-9-PROG. REG.	C 02.04.00.1	V3	
LATCH REGISTER	N 02.30.82.1	V5	DP
MQ REGISTER	C 02.01.00.1	V2	
MQ REGISTER C -WORD EVEN TGR-	C 03.30.02.1	V6	
POSITION REGISTER 14-17	C 02.04.18.1	V3	
POSITION REGISTER 13	N 02.04.18.1	V3	
POSITION REGISTER F - 1A TGR-	C 02.10.55.1	V4	
PROGRAM REGISTER S-9-INSTR.REG.	C 02.04.00.1	V3	

NAME	ALD PAGE	VOL	MFI
PROGRAM REGISTER 24-27	N 02.04.47.1	V3	
SHIFT COUNTER	C 02.04.10.1	V3	
STORAGE REGISTER	C 02.01.00.1	V2	
STORAGE REGISTER 36 -SR C-	C 02.05.36.1	V3	
SWAP REGISTER	N 02.30.82.1	V5	DP
TAG ABC-	C 02.04.20.1	V3	EP
TALLY COUNTER	C 02.20.00.1	V5	SP-OP

TRIGGERS AND MAJOR LINES

NAME	ALD PAGE	VOL	MFI
60 CYCLE BUFFER TGR.	N 02.16.51.1	V4	AT
9 CARRY TGR.	C 02.20.07.1	V5	SP
9 OVERFLOW TGR.	C 02.20.06.1	V5	SP
A1 O1	C 02.15.01.1	V4	
A2 D1	C 02.15.02.1	V4	
A3 DI	C 02.15.03.1	V4	
A4 O1	C 02.15.04.1	V4	
A5 O1	C 02.15.05.1	V4	
AC OVERFLOW TGR.	C 02.10.41.1	V4	
ALPHA EARLY TGR.	C 02.15.33.1	V4	
ALPHA LATE TGR.	N 02.15.33.1	V4	
AO D1	C 02.15.00.1	V4	
BETA CYCLE TGR.-MASTER BETA TGR.	C 02.15.39.1	V4	
BETA EARLY TGR.	C 02.15.33.1	V4	
BETA LATE TGR.	N 02.15.33.1	V4	
BLAST CONTROL TGR.	N 02.13.04.1	V4	
BLOCK TGR.	N 02.15.39.1	V4	
C CYCLE PARITY TRAP REQUEST TGR.	N 02.13.01.1	V4	
C CYCLE REQUEST TGR.	N 02.16.51.1	V4	AT
C EARLY REQUEST TGR.	N 02.16.51.1	V4	AT

NAME	LIGHT	ALD	PAGE	VOL	MF1	NAME	LIGHT	ALD	PAGE	VOL	MF1
C REQUEST INTERLOCK TGR.	N	02.16.51.1	V4	AT		MEMORY PROTECT COMPARE UNEQUAL	N	02.16.04.1	V4	MP	
CHANNEL CHECK A	C	03.30.03.1	V6			MEMORY PROTECT MODE TGR.	C	02.16.05.1	V4	MP	
CHANNEL CHECK BCDE	C	06.15.02.1	V7			MEMORY PROTECT VIOLATION TGR.	N	02.16.05.1	V4	MP	
CHANNEL IN USE A	C	02.10.06.1	V4			MPY ADD RIGHT TGR	N	02.10.21.1	V4		
CHANNEL IN USE BCDE 06.20.02.1	C	02.10.06.1	V7-V4	CH-		MPY-DIV TGR	N	02.10.20.1	V4		
CHANNEL SELECT A	N	02.04.48.1	V3			MQ C -WORD EVEN TGR.-	C	03.30.02.1	V6		
CHANNEL SELECT B	N	02.04.48.1	V3	CHB		DSCILLATOR - CLOCK	N	02.15.17.1	V4		
CHANNEL SELECT C	N	02.04.49.1	V3	CHC		PARTY CHECK-PARTY ERROR TGR.-	C	02.05.45.1	V3		
CHANNEL SELECT D	N	02.04.49.1	V3	CHD		PARTY ERROR TGR.	C	02.05.45.1	V3		
CHANNEL SELECT E	N	02.04.49.1	V3	CHE		PARTY INHIBIT-PARTY MODE TGR-	C	02.13.03.1	V4		
CHANNEL TRAP CONTROL TGR.	C	02.13.03.1	V4			PARTY MODE TGR.-PARTYINHIBIT-	C	02.13.03.1	V4		
CHANNEL TRAP TGR.	N	02.13.06.1	V4			PARTY TRAP TGR.	N	02.13.06.1	V4		
CLASS ADDRESSES	N	02.04.42.1	V3			PARTIAL STORE TGR.	N	02.15.34.1	V4		
CLEAR TGR.	N	02.14.04.1	V4			POD 10. 12. 14. 16. IX. X2	N	02.04.01.1	V3		
CLOCK A0 ~ A1 ~ A2	N	02.15.18.1	V4			POD 24. 26	N	02.04.02.1	V3	SP	
CLOCK GATE TGR.	N	02.15.16.1	V4			POD 20. 22. X4	N	02.04.02.1	V3		
CLOCK OSCILLATOR	N	02.15.17.1	V4			POD 32. 34. 36. X6	N	02.04.03.1	V3		
DIRECT DATA TRAP TGR.	N	02.13.06.1	V4			POD 30	N	02.04.03.1	V3	SP	
DISPLAY STORAGE TGR.	N	02.14.03.1	V4			POD 40. 42	N	02.04.04.1	V3		
DIV CHECK TGR	C	02.10.22.1	V4			POD 53	N	02.04.05.1	V3	EP	
DOUBLE PRECISION FLOAT PT TRAP TN	02.20.41.1	V5		SP		POD 50.52. 54. 56. 5X	N	02.04.05.1	V3		
E CYCLE PARITY TRAP REQUEST TGR	N	02.13.01.1	V4			POD 63	N	02.04.05.1	V3	EP	
E LATE TGR.	N	02.15.30.1	V4			POD 60. 62. 64. 66. 6X	N	02.04.06.1	V3		
EARLY C REQUEST TGR.	N	02.16.51.1	V4	AT		POD 70. 72. 74. 76. 7X	N	02.04.07.1	V3		
END OPERATION	N	02.15.35.1	V4			POD 07	N	02.04.00.1	V3	EP	
END OPERATION TGR.	N	02.15.39.1	V4			POD 00. 02. 06. 0X. XO	N	02.04.00.1	V3		
END OPERATION-FLOATING POINT	N	02.20.09.1	V5	SP		POSITION REGISTER F-1A TGR.-	C	02.10.65.1	V4		
ENTER INSTRUCTION TGR.	N	02.14.03.1	V4			PRE 1A TGR.	N	02.10.65.1	V4		
ENTER STORAGE TGR.	N	02.14.03.1	V4			PRIVILEGED INSTRUCTION TGR.	N	02.13.04.1	V4		
FIRST C CYCLE COMPLETE TGR.	N	02.16.53.1	V4	AT		PROGRAM RESET TGR.	N	02.14.20.1	V4		
FIRST C CYCLE DELAYED TGR.	N	02.16.54.1	V4	AT		PROGRAM STOP TGR.	C	02.14.06.1	V4		
FIRST C LATE TGR.	N	02.16.53.1	V4	AT		PULSE MODE BETA 1D1 DELAYED TGR	N	02.15.16.1	V4		
FIRST E TIME	N	02.15.39.1	V4	DP		PULSE MODE LATCH TGR.	N	02.15.16.1	V4		
FLOATING POINT TRAP TGR.	N	02.13.06.1	V4	SP		Q CARRY TGR.	C	02.10.41.1	V4		
FLOATING POINT 2 TGR.	C	02.20.06.1	V5	DP		READY LIGHT	C	02.14.06.1	V4		
FLOATING POINT 1 TGR.	C	02.20.07.1	V5	SP		RESET I TGR.	N	02.14.04.1	V4		
FLOATING POINT-END OPERATION	N	02.20.09.1	V5	SP		RESET II TGR.	N	02.14.04.1	V4		
FP FLAG 14 TGR.-TRAP REQUEST	N	02.20.40.1	V5	SP		SECOND E TIME	N	02.15.39.1	V4	DP	
FP FLAG 15 TGR.-AC-MO OVERFLOW	N	02.20.40.1	V5	SP		SINGLE CYCLE TGR.	N	02.14.03.1	V4		
FP FLAG 16 TGR.-AC OVER OR UNDERN	N	02.20.40.1	V5	SP		SINGLE INSTRUCTION TGR.	N	02.14.02.1	V4		
FP FLAG 17 TGR.-MQ OVER OR UNDERN	02.20.41.1	V5	SP			SKIP SYNC TGR.	N	02.10.74.1	V4		
GO TO C	N	02.16.52.1	V4	AT		S00	N	02.04.45.1	V3		
GO TO E	N	02.15.34.1	V4			STACKED PARITY TRAP REQUEST TGR	N	02.13.01.1	V4		
GO TO L	N	02.15.34.1	V4	DP		START TGR.	N	02.14.02.1	V4		
HB 111 TGR.-PREVENTS DIV OP.-	N	02.10.22.1	V4			STOP TGR. -MASTER	C	02.14.05.1	V4		
I LATE TGR.	N	02.15.30.1	V4			STOP TGR. -PROGRAM-	C	02.14.06.1	V4		
I OR IA PARITY TRAP REQUEST TGR	N	02.13.01.1	V4			STORAGE BUS	N	02.05.00.1	V3		
IA TGR. -POSITION REGISTER F-	C	02.10.65.1	V4			STORAGE REGISTER 36 -SR C-	C	02.05.36.1	V3		
I-O CHECK TGR.	C	02.10.74.1	V4			STORE CYCLE TGR	N	02.12.50.1	V4		
INSTRUCTION COUNTER OVERFLOW	N	02.14.20.1	V4			TALLY COUNTERS	C	02.20.00.1	V5	SP-DP	
INTERVAL TIMER TRAP TGR.	N	02.13.05.1	V4			TAPE SENSE TGR.	N	02.15.36.1	V4		
IT BLAST REQUEST TGR.	N	02.16.54.1	V4	AT		TMT READ EARLY	N	02.10.90.1	V4	EP	
IT OVERFLOW TGR.	N	02.16.54.1	V4	AT		TMT READ LATE	N	02.10.90.1	V4	EP	
IT OVERFLOW TRAP REQUEST TGR.	N	02.16.54.1	V4	AT		TRAP CONTROL TGR.-TRAP INHIBIT-	C	02.13.03.1	V4		
L LATE TGR.	N	02.15.30.1	V4			TRAP INHIBIT-TRAP CONTROL TGR.-	C	02.13.03.1	V4		
LAST TGR.	N	02.14.04.1	V4			UNITS ADDRESS 6+7+10+11+12+14	N	02.04.41.1	V3		
LOAD 2 TGR.	N	02.14.06.1	V4			UNITS ADDRESS 0-5	N	02.04.40.1	V3		
LOAD TGR.	N	02.14.04.1	V4			X CARRY TGR.	C	02.10.41.1	V4		
MASTER BETA TGR.-BETA CYCLE TGR.	C	02.15.39.1	V4								
MASTER C CYCLE TGR.	N	02.16.52.1	V4	AT							
MASTER E TGR.	C	02.15.30.1	V4								
MASTER I TGR.	C	02.15.30.1	V4								
MASTER L TGR.	C	02.15.30.1	V4								
MASTER STOP TGR.	C	02.14.05.1	V4								
MEMORY PROTECT TRAP TGR.	N	02.13.05.1	V4								

7106 CORE STORAGE UNIT

MFI CODES

A1 4K MEMORIES ONLY
 A2 8K MEMORY ADDITIONS
 A3 16K MEMORY ADDITIONS
 A4 32K MEMORY ADDITIONS

DRIVERS, REGISTERS, AND MAJOR LINES

NAME	LIGHT	ALD	PAGE	VOL	MFI
CLOCK - READ-WRITE	N	01.	10.10.1	V1	
I INHIBIT DRIVERS	N	01.	20.10.1	V1	
MEMORY ADDRESS REGISTER	N	01.	11.07.1	V1	
MEMORY DATA REGISTER	N	01.	19.01.1	V1	
READ-WRITE CLOCK	N	01.	10.10.1	V1	
SENSE AMPLIFIERS	N	01.	18.10.1	V1	
X GATES	N	01.	16.01.1	V1	
X READ DRIVERS	N	01.	14.10.1	V1	
X WRITE DRIVERS	N	01.	14.10.1	V1	
Y GATES	N	01.	17.10.1	V1	
Y READ DRIVERS	N	01.	15.10.1	V1	
Y WRITE DRIVERS	N	01.	15.10.1	V1	

7107 CORE STORAGE UNIT

MFI CODES

B1 8K MEMORIES ONLY
 B2 16K MEMORY ADDITIONS
 B3 32K MEMORY ADDITIONS

DRIVERS, REGISTERS, AND MAJOR LINES

NAME	LIGHT	ALD	PAGE	VOL	MFI
MEMORY ADDRESS REGISTER	N	01.	11.01.1	V1	
MEMORY DATA REGISTER 00-39	N	01.	19.01.1	V1	
MEMORY DATA REGISTER 40-73	N	01.	19.11.1	V1	B4
SENSE AMPLIFIERS 00-37	N	01.	18.01.1	V1	
SENSE AMPLIFIERS 38-76	N	01.	18.10.1	V1	B4
X GATES	N	01.	16.00.1	V1	
X MATRIX SWITCH DECODE	N	01.	12.01.1	V1	
X SELECT GATE DRIVERS	N	01.	16.09.1	V1	
Y DRIVERS	N	01.	15.01.1	V1	
X DRIVERS	N	01.	14.01.1	V1	
Y GATES	N	01.	16.00.1	V1	
Y MATRIX SWITCH DECODE	N	01.	13.01.1	V1	
Y SELECT GATE DRIVERS	N	01.	17.09.1	V1	
Z DRIVERS 36-72	N	01.	20.04.1	V1	B4
Z DRIVERS 00-35	N	01.	20.01.1	V1	

CHANNEL A

MFI CODES

U0 INTERFACE 0 ADAPTER FOR 1414 TAPE
 U3 INTERFACE 3 ADAPTER FOR 1414 CARD MACHINES
 U5 INTERFACE 5 ADAPTER FOR 1401
 UR INTERFACE 3 ADAPTER FOR 1622
 U03 CIRCUITS COMMON TO 1414 TAPE AND 1414 CARD MACHINES
 U05 CIRCUITS COMMON TO 1414 TAPE AND 1401
 U35 CIRCUITS COMMON TO 1414 CARD MACHINES AND 1401
 URO CIRCUITS COMMON TO 1414 TAPE AND 1622
 UR3 CIRCUITS COMMON TO 1414 CARD MACHINE AND 1622
 URO3 CIRCUITS COMMON TO 1414 TAPE, 1414 CARD
 MACHINES, AND 1622
 UR35 CIRCUITS COMMON TO 1414 CARD MACHINES, 1401, AND 1622

TRIGGERS AND MAJOR LINES

NAME	LIGHT	ALD	PAGE	VOL	MFI
I401 ATTENTION TGR. -ENABLE-	N	03.05.	06.1	V6	U5
I401 ATTENTION-ATT SYNC TGR.	P	03.05.	06.1	V6	U5
I401 END TGR.	P	03.05.	06.1	V6	U5
I401 INSTRUCTION TRANSFER	P	03.05.	07.1	V6	U5
I401 READY TGR.	P	03.05.	05.1	V6	U5
I401 SENSE BUSY	P	03.05.	08.1	V6	U5
I401 SENSE INDICATOR TGR.	N	03.05.	09.1	V6	U5
I401 SERVICERESPONSE-IN OR OUT-	P	03.05.	07.1	V6	U0
ALLOW ERROR TGR.	P	03.00.	07.1	V6	U0
ATTENTION SYNC TGR.	N	03.03.	15.1	V6	U3
ATTENTION SYNC TGR.	P	03.05.	06.1	V6	U5
BACKSPACE-REWIND TGR.	P	03.00.	08.1	V6	U0
BINARY MODE TGR.	P	03.10.	06.1	V6	
BLOCK WRITE SOLENOID TGR.	P	03.04.	05.1	V6	
BUFFER ATTENTION TGR.	P	03.03.	15.1	V6	UR3
BUFFER GO TGR.	P	03.03.	10.1	V6	U3
BUSY STATUS TGR.	P	03.00.	10.1	V6	U0
C BIT TRANSLATOR	N	03.30.	05.1	V6	
C1 -STROBE TGR.-	P	03.20.	01.1	V6	
C2 -STROBE TGR.-	P	03.20.	01.1	V6	
C3 -STROBE TGR.-	P	03.20.	01.1	V6	
CARD MACHINE SELECT	N	03.03.	01.1	V6	U3
CARRIER RETURN TGR.	P	03.04.	04.1	V6	
CHANNEL IN OPERATION TGR.	P	03.10.	02.1	V6	
CHANNEL IN USES TGR.	P	03.10.	02.1	V6	
CONTROL TGR.	P	03.10.	05.1	V6	
DISCONNECT DELAY TGR.	P	03.20.	02.1	V6	
DISCONNECT SYNC TGR.	P	03.10.	10.1	V6	
DISCONNECT TGR.	P	03.10.	10.1	V6	
ENABLE ATTENTION TGR.	P	03.30.	06.1	V6	
ENABLE END TGR.	P	03.30.	06.1	V6	
ENABLE PARITY TGR.	P	03.30.	06.1	V6	
ENABLE UNIT RECORD-ENB BU INT T	P	03.30.	06.1	V6	
END OPERATION CONTROL TGR.	P	03.10.	03.1	V6	
END OPERATION TGR.	P	03.10.	03.1	V6	
END SELECT-SELECT END TGR.	P	03.00.	08.1	V6	U0
END TRAP TGR.	P	03.30.	07.1	V6	
END-OF-FILE TGR.	P	03.30.	04.1	V6	
END-OF-RECORD TGR.	P	03.10.	10.1	V6	
END-OF-TAPE TGR.	P	03.30.	04.1	V6	
ERASE CONTROL TGR.	P	03.00.	10.1	V6	U0
FILL MQ TGR.	P	03.10.	11.1	V6	
FIRST CHARACTER TAPEMARK TGR.	P	03.00.	07.1	V6	U0
FORMS DELAY 1 TGR.	P	03.03.	10.1	V6	U3
FORMS DELAY 2 TGR.	P	03.03.	10.1	V6	U3
GO TO U TGR.	P	03.20.	10.1	V6	U3
IN MODE TGR.	P	03.03.	12.1	V6	U3
INHIBIT TGR.	P	03.10.	09.1	V6	
INHIBIT WR. SOLENOID-BLK WR SOL	P	03.04.	05.1	V6	
INITIAL WORD COUNT ZERO TGR.	P	03.10.	06.1	V6	
INITIAL ZERO-INIT WC ZERO TGR.	P	03.10.	06.1	V6	
INSTRUCTION DECODING	N	03.10.	01.1	V6	
INSTRUCTION TRANSFER TGR.	P	03.05.	07.1	V6	U5
INTERFACE 0	N	03.00.	02.0	V6	U0
INTERFACE 1 TGR. -BINARY-	P	03.10.	07.1	V6	
INTERFACE 2 TGR. -BINARY-	P	03.10.	07.1	V6	
INTERFACE 3 WITH 1414 CARD MACH	N	03.03.	30.0	V6	U3
INTERFACE 3 WITH 1622	N	03.03.	31.0	V6	UR
INTERFACE 4	N	03.04.	40.0	V6	
INTERFACE 4 TGR. -BINARY-	P	03.10.	07.1	V6	
INTERFACE 5	N	03.05.	50.0	V6	U5
KA THRU KE INSTRUCTIONS -1401-	N	03.05.	04.1	V6	U5
LAST CARD TGR.	N	03.03.	24.1	V6	UR
MC C-WORD EVEN TGR.-	C	03.30.	02.1	V6	

NAME	LIGHT	ALD	PAGE	VOL	MF1
OUT MODE TGR.	P	03.03.12.1	V6	U3	
OUTPUT RESPONSE TGR.	N	03.05.07.1	V6	U5	
PAPER TAPE READER BUSY TGR. -PTRP	03.03.14.1	V6		UR3	
PARTITY CIRCUITS	N	03.30.01.1	V6		
POSITION 13 EQUAL ONE TGR.	N	03.03.16.1	V6	U3	
POSITION 13 EQUAL ZERO TGR.	N	03.03.16.1	V6	U3	
PRINTER BUSY TGR. -PR-	P	03.03.14.1	V6	UR3	
PUNCH BUSY TGR. -PU-	P	03.03.14.1	V6	UR3	
PUNCH DELAY TGR.	N	03.03.22.1	V6	UR	
READ DELAY 1 TGR.	N	03.03.24.1	V6	UR	
READ DELAY 2 TGR.	N	03.03.24.1	V6	UR	
READ END TGR.	P	03.03.24.1	V6	UR	
READ GATE TGR.	P	03.03.23.1	V6	UR	
READ SERVICE REQUEST TGR.	N	03.03.24.1	V6	UR	
READ TGR.	P	03.10.04.1	V6		
READ TRANSLATOR	N	03.20.04.1	V6		
READER BUSY TGR. -RD-	P	03.03.14.1	V6	UR3	
SELECT 1 TGR.	P	03.03.09.1	V6	U3	
SELECT 2 TGR.	P	03.03.09.1	V6	U3	
SELECT 2 TGR.	P	03.03.09.1	V6	U3	
SELECT 3 TGR.	P	03.03.09.1	V6	U3	
SELECT DATA TRANSMISSION UNIT	TGP	03.03.07.1	V6	U3	
SELECT END TGR.	P	03.00.08.1	V6	U0	
SELECT INTERFACE ZERO TGR.	P	03.10.08.1	V6		
SELECT PAPER TAPE READER TGR	P	03.03.08.1	V6	U3	
SELECT PRINTER TGR.	P	03.03.06.1	V6	U3	
SELECT PUNCH TGR.	P	03.03.07.1	V6	UR3	
SELECT READER TGR.	P	03.03.06.1	V6	UR3	
SELECT REMOTE INQUIRY TGR.	P	03.03.08.1	V6	U3	
SELECT TTY TGR	P	03.03.07.1	V6	U3	
SENSE BUSY TGR.	P	03.05.08.1	V6	U5	
SENSE INDICATOR TGR.	N	03.05.10.1	V6	U5	
SENSE TGR.	P	03.10.05.1	V6		
SERVICE REQUEST PRINT	P	03.04.05.1	V6		
SERVICE REQUEST SPACE	P	03.04.05.1	V6		
SERVICE RESPONSE WRITE TGR.	P	03.03.23.1	V6		
SERVICE RESPONSE -IN OR OUT-	P	03.05.07.1	V6	UR	
SOLENOID DRIVERS	N	03.04.01.1	V6	UR	
SR LOADED TGR.	P	03.20.09.1	V6		
SR REQUEST 1 TGR.	P	03.20.09.1	V6		
SR REQUEST 2 TGR.	P	03.20.09.1	V6		
STROBE C1 TGR.	P	03.20.01.1	V6		
STROBE C2 TGR.	P	03.20.01.1	V6		
STROBE C3 TGR.	P	03.20.01.1	V6		
STROBE GENERATE TGR.	P	03.20.01.	V6		
SYNC 1 TGR.	P	03.20.02.1	V6		
SYNC 2 TGR.	P	03.20.02.1	V6		
TAPE BUSY-BUSY STATUS TGR.	P	03.00.10.1	V6	U0	
TAPE UNIT SELECT 0-9	N	03.00.01.1	V6	U0	
TRANSLATOR-C BIT	N	03.30.05.1	V6		
TRANSLATOR-READ	N	03.20.04.1	V6		
TRANSLATOR-WRITE	N	03.20.05.1	V6		
TRAP PRIORITY TGR.	P	03.30.09.1	V6		
TYPEWRITER CIRCUITS	N	03.04.42.0	V6		
TYPEWRITER DATA REGISTER	N	03.04.06.1	V6		
TYPEWRITER SOLENOID DRIVERS	N	03.04.01.1	V6		
U END TRAP TGR.	P	03.30.10.1	V6		
U LATE TGR.	P	03.20.10.1	V6		
WORD COUNT ZERO TGR.	P	03.10.11.1	V6		
WORD EVEN TGR. -MD C-	C	03.30.02.1	V6		
WORD PARITY TGR.	P	03.30.07.1	V6		
WRITE CALL-WRITE GATE TGR.	P	03.03.23.1	V6	UR	
WRITE END-OF-RECDRD DELAY TGR.	N	03.03.22.1	V6	UR	

NAME	LIGHT	ALD	PAGE	VOL	MF1
RITE END-DF-RECORD TGR.	N	03.03.22.1	V6	UR	
RITE GATE TGR.	P	03.03.23.1	V6	UR	
RITE GATE TGR.	P	03.10.09.1	V6		
RITE SERVICE RESP.-SVC RES WR	P	03.03.23.1	V6	UR	
RITE TGR.	P	03.10.04.1	V6		
RITE TRANSLATOR	N	03.20.05.1	V6		

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1
904 CHANNELS B, C, D, AND E				2	

NAME	LIGHT	ALD	PAGE	VOL	MF1

<tbl_r cells

CORE STORAGE

NAME	LIGHT ALD PAGE	VOL	MFI
DD STATUS TGR	P 06.52.00.I	V7	DD
DIRECT DATA END-OF-RECORD GATE	TP 06.12.15.I	V7	DD
DIRECT DATA INTERFACE	N 06.51.00.I	V7	DD
DISCONNECT CALL TGR.	P 06.20.12.I	V7	
DISCONNECT SYNC TGR.	P 06.16.02.I	V7	
DISCONNECT TGR. -CHANNEL-	P 06.20.13.I	V7	
ENABLE ATTENTION TGR.	P 06.16.00.I	V7	SI
ENABLE COLUMN WORD TRAP TGR.	P 06.16.00.I	V7	
ENABLE DIRECT DATA INTERRUPT TGR	TP 06.16.00.I	V7	DD
ENABLE END-ENB CWT TGR.	P 06.16.00.I	V7	
ENABLE PARITY-ENB TCT TGR.	P 06.16.00.I	V7	
ENABLE TAPE CHECK TRAP TGR.	P 06.16.00.I	V7	
END RESPONSE TGR.	P 06.20.29.I	V7	SI
END-OF-FILE SYNC TGR.	P 06.16.02.I	V7	TIDD
END-OF-FILE TGR.	P 06.15.01.I	V7	TIDD
FIRST B CYCLE-WRITE FIRST B CYCLP	06.20.27.I	V7	
FIRST BINARY-AWAIT FIRST BIN CHAP	06.20.27.I	V7	TI
FIRST CHARACTER TAPEMARK TGR.	P 06.15.01.I	V7	TI
INTERFACE 1414	N 06.03.01.0	V7	TI
INTERFACE DIRECT DATA	N 06.51.00.I	V7	DD
INTERFACE SIMPLEX	N 06.40.00.I	V7	SI
IO-MF END OPERATION TGR.	P 06.20.01.I	V7	
PARITY GENERATOR	N 06.18.00.I	V7	TISI
PROGRAM INDICATOR SYNC TGR.	P 06.15.04.I	V7	
READ LAST WORD TGR.	P 06.20.14.I	V7	TISI
READ PARITY GENERATOR TGR.	P 06.1B.01.I	V7	TISI
READ SELECT TGR.	P 06.20.00.I	V7	
READ TRANSLATOR	N 06.11.02.I	V7	TISI
REDUNDANCY CHECK TGR.	P 06.15.02.I	V7	
REDUNDANCY CHECK-CONSOLE BCDE	C 06.15.02.I	V7	
REDUNDANCY CHECK SYNC TGR.	P 06.16.02.I	V7	
SERVICE RESPONSE TGR.	P 06.20.25.I	V7	SI
SIMPLEX INTERFACE	N 06.40.00.I	V7	SI
SIMPLEX INTERFACE SELECT TGR.	P 06.40.02.I	V7	
SIXTH CHARACTER TGR.	P 06.20.25.I	V7	
STOP TGR.	P 06.20.27.I	V7	SI
TAPE END TGR.	P 06.15.00.I	V7	
TAPE SELECT TGR.	P 06.30.00.I	V7	TI
TAPE UNIT SELECT 0-9	N 06.30.01.I	V7	TI
TI SI BUSY TGR.	P 06.20.12.I	V7	TISI
TRANSLATOR-READ	N 06.11.02.I	V7	TISI
TRANSLATOR-WRITE	N 06.11.05.	V7	TISI
TRANSMISSION LOSS TGR.	P 06.20.10.I	V7	
TRAP PRIORITY TGR.	P 06.16.03.I	V7	
TRIGGER 14 TGR.	P 06.40.02.I	V7	
UNUSUAL END SYNC TGR.	P 06.16.01.I	V7	
UNUSUAL END TGR.	P 06.20.29.I	V7	
WORD COUNT ZERO	P 06.12.15.I	V7	
WORD PARITY ERROR TGR.	P 06.1B.02.I	V7	
WORD PARITY SYNC TGR.	P 06.16.01.I	V7	
WRITE FIRST B CYCLE TGR.	P 06.20.27.I	V7	
WRITE FIRST WORD TGR.	P 06.20.24.I	V7	TISI
WRITE ODD COUNT TGR.	P 06.1B.02.I	V7	TISI
WRITE SELECT TGR.	P 06.20.00.I	V7	
WRITE TRANSLATOR	N 06.11.05.I	V7	TISI

MEMORY PROTECT

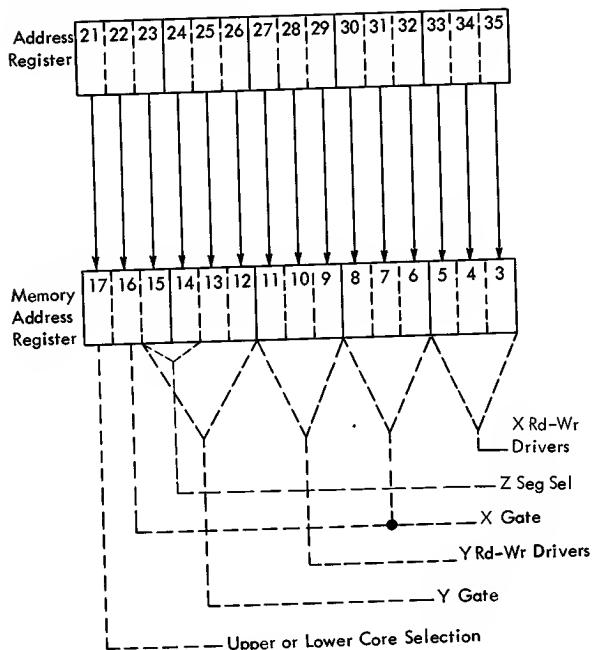
The number of locations protected:

33 to 35	32 = 1	32 = 0
Count Register	Trap* on Equal	Trap* on Unequal
7	400 ₈	77,400 ₈
	1,000 ₈	77,000 ₈
	2,000 ₈	76,000 ₈
	4,000 ₈	74,000 ₈
3	10,000 ₈	70,000 ₈
2	20,000 ₈	60,000 ₈
1	40,000 ₈	40,000 ₈
0	100,000 ₈	0 ₈

* Memory is protected when machine traps.

7106 CORE STORAGE

7106 MAR Bit Arrangement



7106 MAR Bit Arrangement

Card Locations

	32	X-Y Gate Driver Load Resistors		1	
A	28	X Gate Dr	13 ← 00	1	
		Odd # Cards - L16K	Even # Cards - U16K		
B	18	15/14	Y Gate Dr 06 ← 00	1	
		X Gates	Odd # Cds - L16K		
	14 and 15		Even # Cds - U16K		
C	18	Y Gate Dr 15 ← 07	1		
		Odd # Cards - L16K			
	Even # Cards - U16K				
D	24	11 ← 00	1		
		Preamps			
E	24	11 ← 00	1		
		Z Drivers			
F	24	23 ← 12	1		
		Preamps			
G	24	23 ← 12	1		
		Z Drivers			
H	27	36 ← 24	2		
		Preamps			
J	27	36 ← 24	2		
		Z Drivers			
K					
A	26	23	22	MDR	
	MAR	36 ← 00	13	10 19 ← 00	1
				Final Amps	
B				9 36 ← 20	1
C				Final Amps	
D					
E	24	11 ← 00	1		
		Preamps			
F	24	11 ← 00	1		
		Z Drivers			
G	24	23 ← 12	1		
		Preamps			
H	24	23 ← 12	1		
		Z Drivers			
J	27	36 ← 24	2		
		Preamps			
K	27	36 ← 24	2		
		Z Drivers			

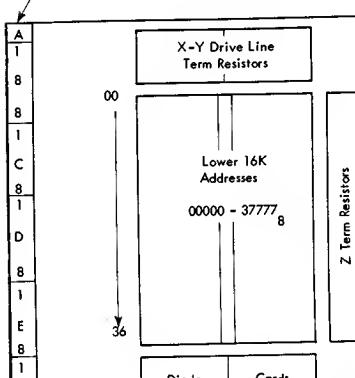
L = Lower Addresses

(00000₈ to 37777₈)

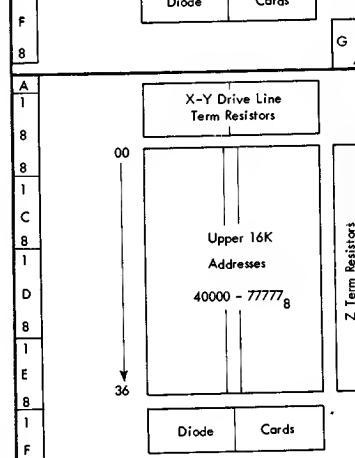
U = Upper Addresses

(40000₈ to 77777₈)

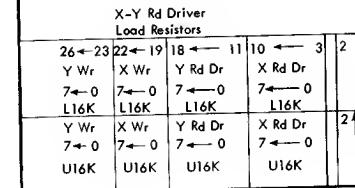
Slide Connectors (Paddle) for X-Y Lines, Sense Windings and Z Drive Lines to Arrays



Panel 1



Panel 3



H

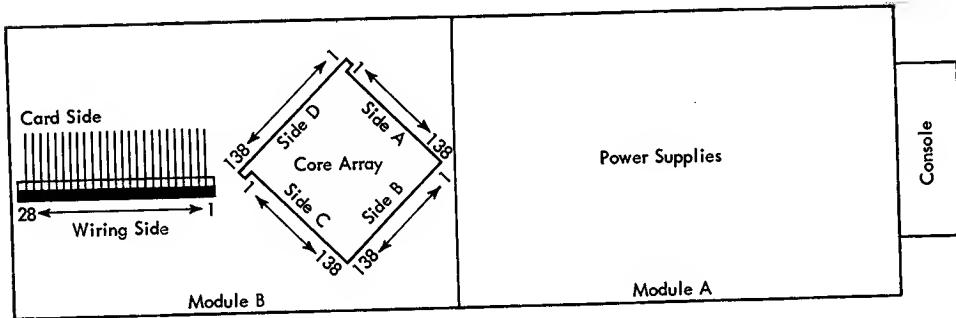
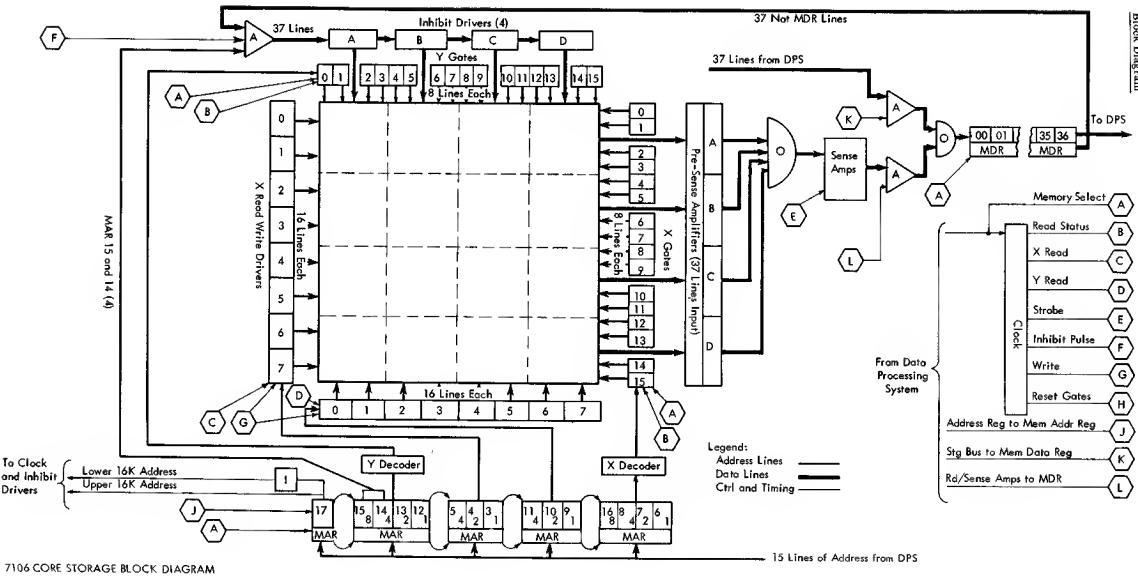
J

K

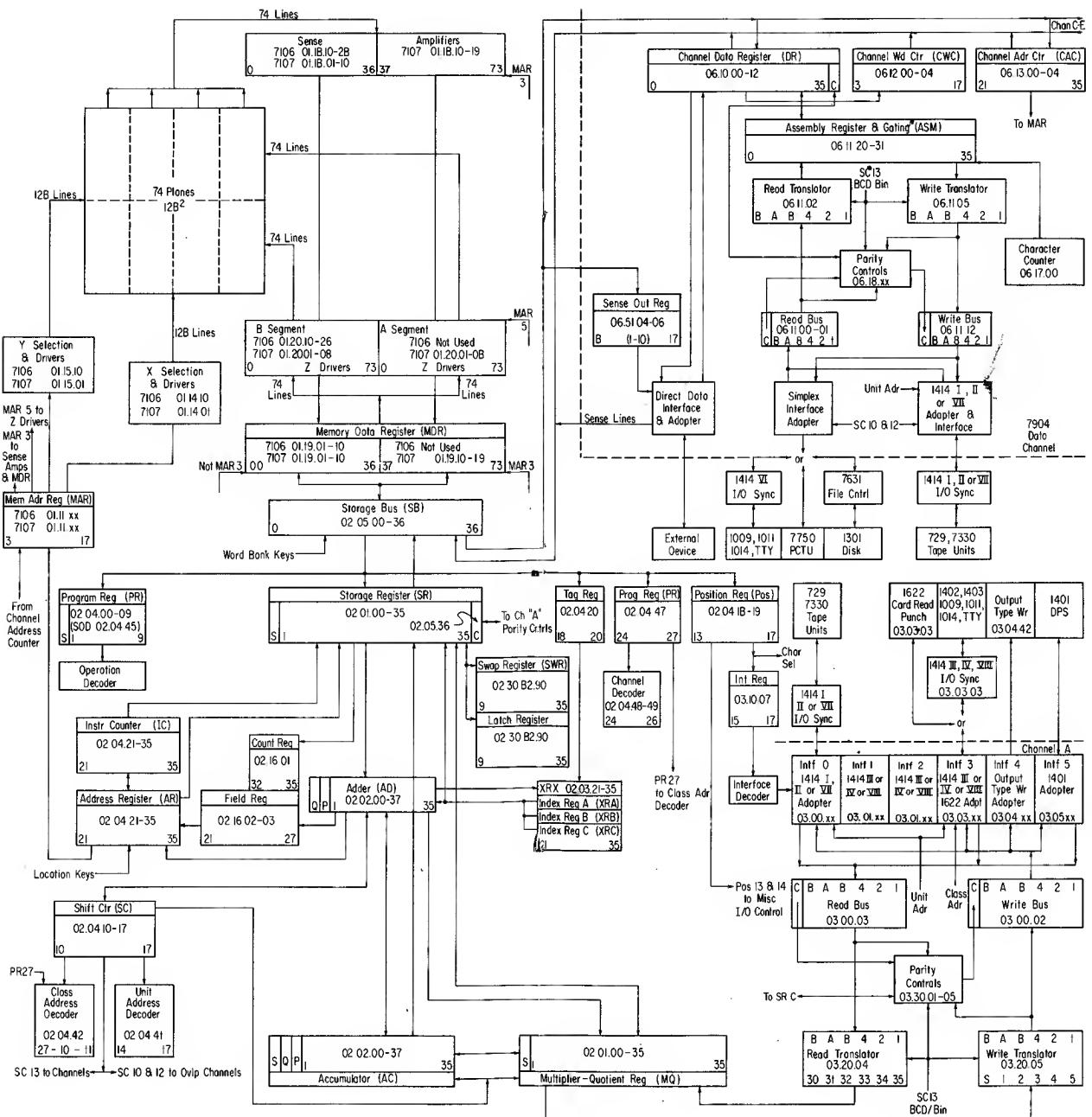
Slide Connections for X-Y Rd-Wr Drivers to Lower Array

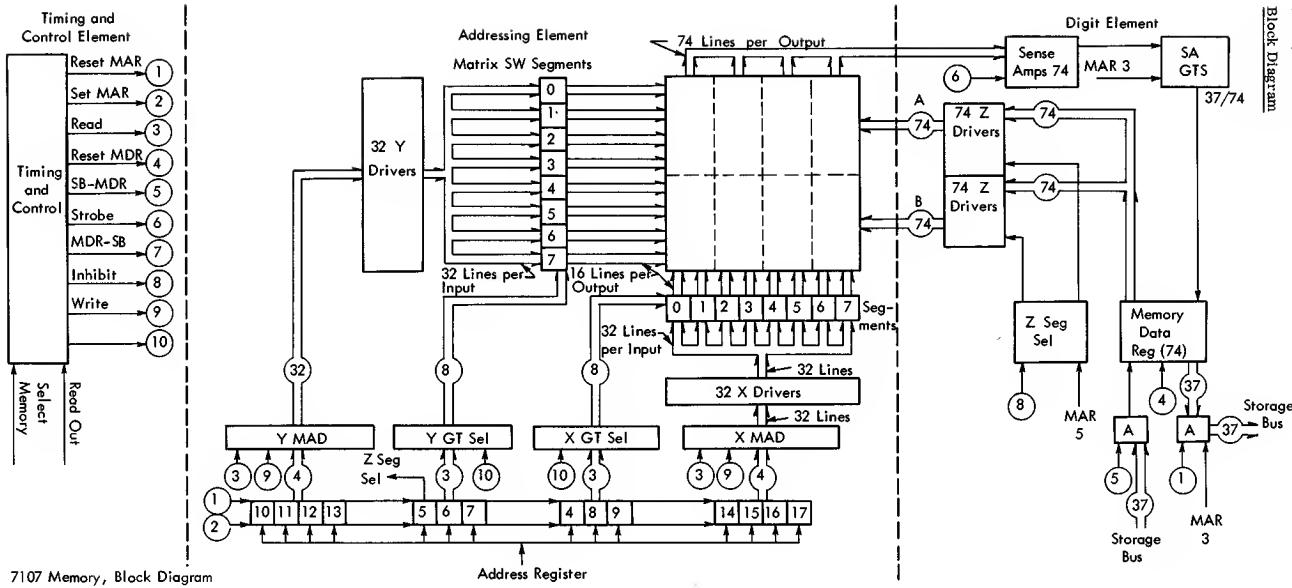
Physical Layout

Photographs showing the physical layout of the 7106 Core Storage are in the 7106 Core Storage Customer Engineering Instruction-Reference Manual.

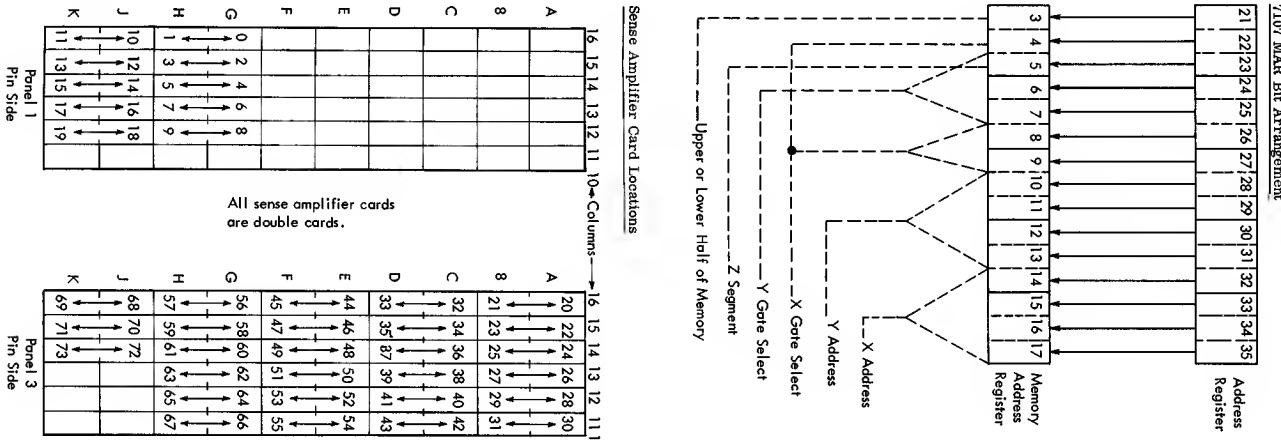


7106 Physical Layout





7107 Memory, Block Diagram



First Level MAD Decoding

X or Y Address	MAD Levels Active					
0000	2	4	6	8	10	12
0001	1	3	5	8	10	12
0010	1	4	6	7	9	12
0011	2	3	5	7	9	12
0100	2	3	6	7	10	11
0101	1	4	5	7	10	11
0110	1	3	6	8	9	11
0111	2	4	5	8	9	11
1000	2	4	5	8	9	11
1001	1	3	6	8	9	11
1010	1	4	5	7	10	11
1011	2	3	6	7	10	11
1100	2	3	5	7	9	12
1101	1	4	6	7	9	12
1110	1	3	5	8	10	12
1111	2	4	6	8	10	12

X Addresses
Memory Address Register Positions 14, 15, 16, and 17

Y Addresses
Memory Address Register Positions 10, 11, 12, and 13

Second Level MAD

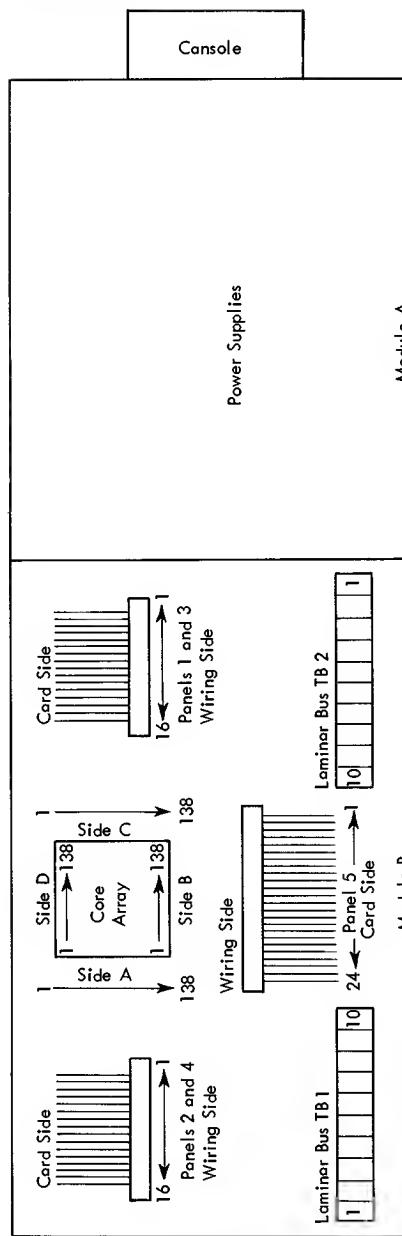
The output of the second level MAD circuits are primary 16 pairs. One line of each pair is active during read, while the other line is active during write. Which line of the pair is active for read or write is determined by first and second level MAD switching. The output lines are numbered 1 through 16 and NOT 1 through NOT 16. Hence, either 1 or NOT 1, 2 or NOT 2, etc. is active for each read. If 1 is active at read time, then NOT 1 is active at write time.

The following chart shows the lines 1 through 16 that are active during read time.

Second Level MAD Decoding - Read

X or Y Address	MAD Primary Levels Active for Read															
0000	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0001	0	N2	3	N4	5	N6	7	N8	9	N10	11	N12	13	N14	15	N16
0010	1	2	N3	N4	5	6	N7	N8	9	10	N11	N12	13	14	N15	N16
0011	1	N2	N3	4	5	N6	N7	8	9	N10	N11	12	N13	N14	N15	16
0100	1	2	3	4	N5	N6	N7	N8	9	N10	N11	12	N13	N14	N15	N16
0101	1	N2	3	N4	N5	6	N7	8	N9	N10	N11	N12	N13	N14	N15	N16
0110	1	2	N3	N4	N5	N6	7	N8	N9	10	N11	12	N13	14	N15	16
0111	1	N2	N3	4	N5	6	N7	N8	N9	N10	N11	12	N13	N14	15	16
1000	1	2	3	4	5	6	7	8	N9	10	11	N12	N13	14	15	N16
1001	1	N2	3	N4	5	N6	N7	N8	N9	N10	N11	12	N13	N14	N15	16
1010	1	2	N3	N4	5	6	N7	N8	N9	N10	11	12	N13	N14	15	16
1011	1	N2	N3	4	5	N6	N7	8	N9	10	11	N12	N13	14	15	N16
1100	1	2	3	4	N5	N6	N7	N8	N9	N10	N11	N12	13	14	15	16
1101	1	N2	3	N4	N5	6	N7	8	N9	10	N11	12	13	N14	15	N16
1110	1	2	N3	N4	N5	N6	7	8	N9	N10	11	12	13	14	N15	N16
1111	1	N2	N3	4	N5	6	7	N8	N9	10	11	N12	13	N14	N15	16

Physical Layout



7107 Physical Layout

POWER SUPPLY

TEST POINTS AND TOLERANCES

Power Supply	Check at Laminar Bus Terminal	Tolerance * * *	Ripple
Frame B			
+60v	7*, 8*, 8	**	0.60v
-32v	5*	± 2.56v	---
+12v	5, 4*	± 0.48v	0.12v
+12v Z	7	± 0.48v	0.12v
-12v M	6*	± 0.48v	0.12v
-12v	4, 6, 3*	± 0.48v	0.12v
+6v	3, 2*	± 0.24v	0.06v
-6v	2	± 0.24v	0.06v
Frames C, D, and E			
+12	5	± 0.48v	0.12v
+12	6	± 0.48v	0.12v
-12 M	9	± 0.48v	0.12v
-12	10	± 0.48v	0.12v
+6	1	± 0.24v	0.06v
+6	2	± 0.24v	0.06v

* Denote 7044 terminal designations.

** Refer to 7040/7044 Core Storage Manual for recommendations.

*** Tolerance includes ripple

	2B	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	B	7	6	5	4	3	2	1
B	Enb Att	Enb Unit Rcd	Enb Par	Enb End				Inh	Wr Gate		EOF	EOT					Bin Mode		Read	Write	Sen	Ctrl		IFR 4	IFR 2	IFR 1		
	30.06	30.06	30.06	30.06				10.09	10.09		30.04	30.04					10.06		10.04	10.04	10.05	10.05		10.7	10.7	10.7		
C		Ward Por	End Trop		Strobe Gen	C1	C2	Sync 1	Sync 2							Fill MQ		Carr Ret	Inh Wr Sol	SVC Req PR	SVC Req SP			Sel IF 0				
		30.07	30.07		20.01	20.01	20.01	20.01	20.02	20.02						10.11		04.04	04.05	04.05	04.05			10.08				
D	Trap PRI		U End Trop		Disc Dly	Disc Sync	Disc		Ch In Use	Ch in Oper		End Op Ctl	End Op			WC Zero	Init Zero		SR Req 1	SR Req 2		SR LDD		GO to U	U Late			
			30.09		30.10			20.02	10.10	10.10		10.02	10.02			10.03	10.03		10.11	10.06		20.09	20.09		20.09	20.10	20.10	

→ EOR
Word Even
RC

D17Q
F17Q
A15Q

10.10
30.02
30.03

01D4
(03.XX.YY.1)

Nome
Name
Name
MFI
Page

										1401	1401		Allow	Busy	Form	Form		Rd	PU	PR	PTR		Sel	Sel	Sel												
B										Sense	End		Error	Status	Dly 1	Dly 2		Busy IF-3	Busy IF-3	Busy IF-3	Busy IF-3		Pch	Print	Rdr												
										U5	U5		U0	U0	U3	U3		UR3	UR3	UR3	UR3		UR3	U3	UR3												
										05.08	05.06		00.07	00.10	03.10	03.10		03.14	03.14	03.14	03.14		03.07	03.06	03.06												
C										1401	1401		Bksp	Sel	Write	1622		Unit	Reed	Int			Sel	Sel	Sel												
										SVC	Att		Rew	End	Coll	1622		Rcd	End	IF-3	IF-3		PTT	RTTY	DTU												
										Resp	U5		U0	U0	UR	03.23		Int	UR3	UR3	UR3		U3	U3	U3												
										05.07	05.06		00.08:1	00.08				03.24	03.23	03.15			03.08	03.08	03.07	03.07											
D										1401	1401		Erase	1st	1622	1622		Buf	Wr	Rd	Gate	SVC		Sel	Sel	Sel											
										Inst	Rdy		Ctl	Char	1622	1622		Att	Buf	Att	Buf	Att		3	2	1											
										Tro	U5		U0	U0	UR	03.23		UR3	03.23	03.15	03.15		U3	U3	U3												
										05.07	05.05		00.10	00.07									03.09	03.09	03.09	03.09											
										2B	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	B	7	6	5	4	3	2	1

J																													
01E4																													
U1, U2																													
Feature Only																													
03.XX.YY.1	2B	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	B	7	6	5	4	3	2	1	

Logic Page	Line In	Input	CPU Line Name	1414-I, II Line Name	Output	Line Out	Logic Page
03.00.01.1	+B	01E3J19D	-C Sel Unit 10	-C Unit Nu 0 to TAU	14D1C04A	+S	60.6B.50.1
03.00.01.1	+B	01E3J19Y	-C Sel Unit 1	-C Unit Nu 1 to TAU	14D1C04C	+S	60.6B.50.1
03.00.01.1	+B	01E3J19G	-C Sel Unit 2	-C Unit Nu 2 to TAU	14D1C04L	+S	60.6B.50.1
03.00.01.1	+B	01E3J19X	-C Sel Unit 3	-C Unit Nu 3 to TAU	14D1C04B	+S	60.6B.51.1
03.00.01.1	+B	01E3J19L	-C Sel Unit 4	-C Unit Nu 4 to TAU	14D1C05A	+S	60.6B.51.1
03.00.01.1	+B	01E3J19G	-C Sel Unit 5	-C Unit Nu 5 to TAU	14D1C05C	+S	60.6B.51.1
03.00.01.1	+B	01E3J19P	-C Sel Unit 6	-C Unit Nu 6 to TAU	14D1C05L	+S	60.6B.52.1
03.00.01.1	+B	01E3J19S	-C Sel Unit 7	-C Unit Nu 7 to TAU	14D1C05B	+S	60.6B.52.1
03.00.01.1	+B	01E3J19B	-C Sel Unit 8	-C Unit Nu 8 to TAU	14D1C06A	+S	60.6B.52.1
03.00.01.1	+B	01E3J19V	-C Sel Unit 9	-C Unit Nu 9 to TAU	14D1C06C	+S	60.6B.53.1
03.00.04.1	+B	01E3J17L	-C Write Call	-C Write Tape Coll	14D1A20L	+S	60.6B.30.1
03.00.04.1	+B	01E3J17Y	-C Read Coll	-C Read Tape Coll	14D1A20B	+S	60.6B.30.1
03.00.04.1	+B	01E3J17X	-C Bksp Call	-C Backspace Call	14D1A20A	+S	60.6B.30.1
03.00.04.1	+B	01E3J17G	-C Wr EOF Call	-C Write Tape Mk Call	14D1A20C	+S	60.6B.30.1
03.00.04.1	+B	01E3J08G	-C Erase Coll	-C Erase Call	14D1A21B	+S	60.6B.31.1
03.00.04.1	+B	01E3J17S	-C REW Call	-C Rewind Coll	14D1A21A	+S	60.6B.31.1
03.00.04.1	+B	01E3J17V	-C RUN Coll	-C Rewind Unload	14D1A21C	+S	60.6B.31.1
03.00.04.1	+B	01E3J17B	-C Turn Off TI	-C Turn Off Tape Ind	14D1A21L	+S	60.6B.31.1
03.00.04.1	+B	01E3J17X	-C Reset TAU	-C Comp Reset to Tape	14D1A22B	+S	60.6B.31.1
03.00.04.1	+B	01E3J17D	-C Disc Coll	-C Disconnect Coll	14D1A22A	+S	60.6B.32.1
03.00.04.1	+B	01E3J17P	-C Bin Mode	-C Odd Parity Op to TAU	14D1A22C	+S	60.6B.32.1
03.00.04.1	+B	01E3J17G	-C Set Tape Sel	-C Set Tape Sel Reg	14D1C06B	+S	60.6B.53.1
03.00.04.1	+B	01E3J1BY	-C Reset Tape Sel	-C Reset Tape Sel Reg	14D1C06L	+S	60.6B.53.1
03.00.02.1	+B	01E3J18G	-C TAU Wr Bus 1	-C CPU to TAU 1 Bit	14D1A06B	+S	60.6B.20.1
03.00.02.1	+B	01E3J18L	-C TAU Wr Bus 2	-C CPU to TAU 2 Bit	14D1A06A	+S	60.6B.20.1
03.00.02.1	+B	01E3J18P	-C TAU Wr Bus 4	-C CPU to TAU 4 Bit	14D1A06C	+S	60.6B.20.1
03.00.02.1	+B	01E3J18B	-C TAU Wr Bus B	-C CPU to TAU B Bit	14D1A06L	+S	60.6B.20.1
03.00.02.1	+B	01E3J18D	-C TAU Wr Bus A	-C CPU to TAU A Bit	14D1A11B	+S	60.6B.21.1
03.00.02.1	+B	01E3J1BS	-C TAU Wr Bus B	-C CPU to TAU B Bit	14D1A11A	+S	60.6B.21.1
03.00.02.1	+B	01E3J1BV	-C TAU Wr Bus C	-C CPU to TAU C Bit	14D1A11C	+S	60.6B.21.1

Logic Page	Line In	Input	1414-I, II Line Name	CPU Line Name	Output	Line Out	Logic Page
60.6B.40.1	-S	14D1D08D	-C TAU to CPU 1 Bit	-C Rd Bus 1	01E3J16A	-B	03.00.03.1
60.6B.40.1	-S	14D1D08C	-C TAU to CPU 2 Bit	-C Rd Bus 2	01E3J16D	-B	03.00.03.1
60.6B.40.1	-S	14D1D08B	-C TAU to CPU 4 Bit	-C Rd Bus 4	01E3J16G	-B	03.00.03.1
60.6B.40.1	-S	14D1D08F	-C TAU to CPU B Bit	-C Rd Bus B	01E3J16L	-B	03.00.03.1
60.6B.40.1	-S	14D1D07D	-C TAU to CPU A Bit	-C Rd Bus A	01E3J16P	-B	03.00.03.1
60.6B.40.1	-S	14D1D07C	-C TAU to CPU B Bit	-C Rd Bus B	01E3J16U	-B	03.00.03.1
60.6B.40.1	-S	14D1D07B	-C TAU to CPU C Bit	-C Rd Bus C	01E3J16X	-B	03.00.03.1
60.6B.41.1	-S	14D1D05F	-C Tape Error	-C Tape Errar	01E3H15C	+B	03.00.05.1
60.6B.41.1	-S	14D1D05C	-C Tape Read Strabe	-C Tape Read Strabe	01E3J15D	-B	03.00.05.1
60.6B.41.1	-S	14D1D04B	-C Select at Load Paint	-C Sel and Ld Pt	01E3J15G	-B	03.00.05.1
60.6B.40.1	-S	14D1D07F	-C Tape Write Strobe	-C Tape Write Strobe	01E3J162	-B	03.00.05.1
60.6B.41.1	-S	14D1D04D	-C Tape Ready	-C Tape Ready	01E3J15L	-B	03.00.05.1
60.6B.40.1	-S	14D1D05D	-C Write Condition	-C Write Cond	01E3J15P	-B	03.00.05.1
60.6B.41.1	-S	14D1D04C	-C Select and Rewind	-C Sel and Rew	01E3J15X	-B	03.00.05.1
60.6B.41.1	-S	14D1D04F	-C Select and Tape Ind On	-C Sel and T I	01E3J15U	-B	03.00.05.1
60.6B.41.1	-S	14D1D05B	-C Tape Busy	-C TAU Busy	01E3J15A	-B	03.00.05.1

Logic Page	Line In	Input	CPU Line Name	1414-IV Line Name	Output	Line Out	Logic Page
03.03.01.1	+B	01E3J06D	-C Sel Reader	-C Unit 1 Select to I-O	14A4K25B	+S	51.40.01.1
03.03.01.1	+B	01E3J03G	-C Sel Printer	-C Unit 2 Select to I-O	14A3D21B	+S	53.50.04.1
03.03.01.1	+B	01E3J08V	-C Sel Pu BCD	-C Unit 4 Select to I-O	14A4K25A	+S	51.40.01.1
03.03.01.1	+B	01E3J0BS	-C Sel Pu Bin	-C Unit B Select to I-O	14A4K21L	+S	51.40.01.1
03.03.01.1	+B	01E3J06G	-C Sel 0 to Buf	-C Select No 0 to Buf	14A4K1BB	+S	51.40.07.1
03.03.01.1	+B	01E3J06L	-C Sel 1 to Buf	-C Select No 1 to Buf	14A4K1BA	+S	51.40.07.1
03.03.01.1	+B	01E3J06P	-C Sel 2 to Buf	-C Select No 2 to Buf	14A4K1BC	+S	51.40.07.1
03.03.01.1	+B	01E3J06B	-C Sel 3 to Buf	-C Select No 3 to Buf	14A4K1BL	+S	51.40.07.1
03.03.01.1	+B	01E3J03P	-C Sel DTU	-C Select Unit D	14A4K17B	+S	51.40.03.1
03.03.01.1	+B	01E3J03B	-C Sel TTY	-C Select Unit L	14A4K19B	+S	51.40.03.1
03.03.01.1	+B	01E3J03S	-C Sel PT Read	-C Select Unit P	14A4K19C	+S	51.40.03.1
03.03.01.1	+B	01E3J03V	-C Sel Rem Ind	-C Select Unit Q	14A4K19L	+S	51.40.03.1
03.03.02.1	+B	01E3J05S	-C Computer Reset	-C Comp Reset to Buf	14A4K21C	+S	52.11.01.1
03.03.02.1	+B	01E3J06G	-C Res Sel Buf	-C Reset Select Buf Ltc	14A4K24A	+S	51.11.01.1
03.03.02.1	+B	01E3J06Y	-C Input Mode	-C Input Mode to Buf	14A4K21B	+S	51.40.02.1
03.03.02.1	+B	01E3J06X	-C Output Mode	-C Output Mode to Buf	14A4K21A	+S	51.40.02.1
03.03.02.1	+B	01E3J03Y	-C Ready to Buffer	-C Ready to Buffer	14A4K25L	+S	51.40.04.1
03.03.02.1	+B	07E3J06G	-C Correct Tran to Buf	-C Corr Trans to Buf	14A4K24B	+S	51.40.04.1
03.03.02.1	+B	01E3J03X	-C Forms Go	-C Forms Stacker Go	14A4K24L	+S	51.40.50.1
03.03.02.1	+B	01E3J03L	-C Forms Control	-C Forms Ctrl to Buf	14A3D21A	+S	53.50.04.1
03.03.03.1	+B	01E3J05C	-C 1414 Wr Bus 1	-C CPU to I-O Sync 1 Bit	14A2K26A	+S	51.40.10.1
03.03.03.1	+B	01E3J05L	-C 1414 Wr Bus 2	-C CPU to I-O Sync 2 Bit	14A2K26C	+S	51.40.10.1
03.03.03.1	+B	01E3J05P	-C 1414 Wr Bus 4	-C CPU to I-O Sync 4 Bit	14A2K26L	+S	51.40.10.1
03.03.03.1	+B	01E3J05B	-C 1414 Wr Bus B	-C CPU to I-O Sync B Bit	14A2K25B	+S	51.40.10.1
03.03.03.1	+B	01E3J05D	-C 1414 Wr Bus A	-C CPU to I-O Sync A Bit	14A2K25A	+S	51.40.10.1
03.03.03.1	+B	01E3J05Y	-C 1414 Wr Bus B	-C CPU to I-O Sync B Bit	14A2K25C	+S	51.40.10.1
03.03.03.1	+B	01E3J05X	-C 1414 Wr Bus C	-C CPU to I-O Sync C Bit	14A2K25L	+S	51.40.10.1

Logic Page	Line In	Input	1414-IV Line Name	CPU Line Name	Output	Line Out	Logic Page
51.40.18.1	-S	14A4K23C	-C Buffer Ready	-C Buffer Ready	01E3H12F	+B	03.03.04.1
51.40.19.1	-S	14A4K15D	-C Reader Busy	-C 1414 Rd Busy	01E3J04A	-B	03.03.14.1
51.40.19.1	-S	14A4K15C	-C Punch Busy	-C 1414 Pu Busy	01E3J04D	-B	03.03.14.1
51.40.19.1	-S	14A4K23D	-C Buffer Busy	-C Buffer Busy	01E3H12D	+B	03.03.04.1
53.50.03.1	-S	14A3D06F	-C 1403 Print Buffer Busy	-C 1414 Pr Busy	01E3J04G	-B	03.03.14.1
51.40.19.1	-S	14A4K15B	-C Paper Tape Reader Busy	-C Prtr Busy	01E3J04L	-B	03.03.14.1
53.50.03.1	-S	14A3D06B	-C Forms Busy Sto to CPU	-C Forms Busy	01E3H15F	+B	03.03.04.1
52.13.03.1	-S	14A4K22F	-C Read Column Binary	-C Read Column Binary	01E3H15G	+B	03.03.04.1
51.40.12.1	-S	14A4K22D	-C Buffer End of Trans	-C Buffer End of Trans	01E3J04U	-B	03.03.05.1
51.40.12.1	-S	14A4K20C	-C Buffer No Trans Cond	-C Buffer No Trans Cond	01E3H12G	+B	03.03.04.1
51.40.02.1	-S	14A4K22B	-C Buffer Inq Out Pulse	-C Buffer Outquiry	01E3J04P	-B	03.03.04.1
51.40.20.1	-S	14A4K23B	-C Buffer Conditions	-C Buffer Conditions	01E3H12C	+B	03.03.04.1
51.40.20.1	-S	14A4K20D	-C Buffer Inq Request	-C Buffer Inquiry	01E3H15H	+B	03.03.04.1
51.40.21.1	-S	14A4K23F	-C Buffer Error	-C Buffer Error	01E3H12E	+B	03.03.04.1
51.40.43.1	-S	14A4K22C	-C Buffer Strobe	-C Buffer SVC Req	01E3H12E	+B	03.03.04.1
51.40.11.1	-S	14A2K24D	-C I-O Sync to CPU 1 Bit	-C 1414-1622 Rd Bus 1	01E3J04X	-B	03.03.05.1
51.40.11.1	-S	14A2K24C	-C I-O Sync to CPU 2 Bit	-C 1414-1622 Rd Bus 2	01E3J07A	-B	03.03.03.1
51.40.11.1	-S	14A2K24B	-C I-O Sync to CPU 4 Bit	-C 1414-1622 Rd Bus 4	01E3J07D	-B	03.03.03.1
51.40.11.1	-S	14A2K24F	-C I-O Sync to CPU B Bit	-C 1414-1622 Rd Bus B	01E3J07L	-B	03.03.03.1
51.40.11.1	-S	14A2K23D	-C I-O Sync to CPU A Bit	-C 1414-1622 Rd Bus A	01E3J07P	-B	03.03.03.1
51.40.11.1	-S	14A2K23C	-C I-O Sync to CPU B Bit	-C 1414-1622 Rd Bus B	01E3J07U	-B	03.03.03.1
51.40.11.1	-S	14A2K23B	-C I-O Sync to CPU C Bit	-C 1414-1622 Rd Bus C	01E3J07X	-B	03.03.03.1

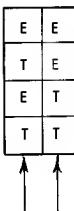
731 INPUT - OUTPUT DEVICE

The 731 console printers used on the 1410 and 7040/44 systems are interchangeable.

731 Type Arrangement A - Report Writing

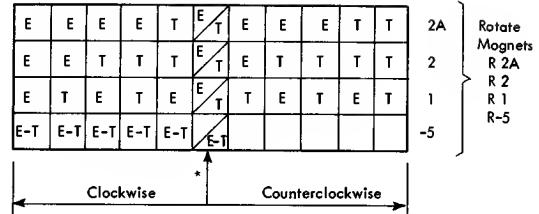
Upper Case													
Tilt	0	█	█	@	>	█	b	█	:	✓	█	-	
1	█	█	%	＼	█	█	█	~	#	█	█		
2	█	█	:=	;	█	-	█] △	█	█	█		
3	█	█	□	<	█	█	█	[丰	█	█	█	↙	
	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5		

Home



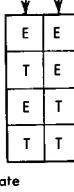
731 Select Latch Chart

Rotate → -5 -4 -3 -2 -1 0 +1 +2 +3 +4 +5



Lower Case													
Tilt	0	1	3	5	7	8	Ø	2	4	6	9	#	
1	/	T	V	X	Y	‡	S	U	W	Z	,		
2	J	L	N	P	Q	I	K	M	O	R	\$		
3	A	C	E	G	H	?	8	D	F	I	.		
	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5		

Home

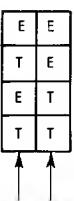


731 Type Arrangement H - Program Language

The type H head is used for FORTRAN and programming the 7040/44 system.

Upper Case													
Tilt	0	█	█	'	>	█	b	█	:	✓	█	-	
1	█	█	(＼	█	█	█	~	#	█	█		
2	█	█	:=	;	█	-	█] △	█	█	█		
3	█	█)	<	█	+	█	[丰	█	█	█	↙	
	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5		

Home



Lower Case													
Tilt	0	1	3	5	7	8	Ø	2	4	6	9	=	
1	/	T	V	X	Y	‡	S	U	W	Z	,		
2	J	L	N	P	Q	!	K	M	O	R	\$		
3	A	C	E	G	H	?	8	D	F	I	.		
	-5	-4	-3	-2	-1	0	+1	+2	+3	+4	+5		

Home

8 = Tilt 2

A = Tilt 1

2 = Rotate +1

4 or 8 = Rotate +1

4 and 8 = Rotate +2A

8 and T, 8 and 1 = Rotate -5

8	A	Tilt
0	0	0
0	1	1
1	0	2
1	1	3

8	A	Rotate
0	0	0 (Home)
0	0	-5
0	0	+1
0	0	-4
0	1	+2
0	1	-3
0	1	+3
0	1	-2
1	0	-1
1	0	+4
1	0	0 (Home)
1	0	+5
1	1	-3
1	1	+2
1	1	-2
1	1	+3

28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	Tape Sel	SI Sel	DD Sel		Chan WRS	Chan Rds	Crtl Sense	BCD Mode	Bksp'd	TI SI Busy	Chan Busy	I/O/MF End Op	DD EOR Gate DD	Wd Ctr = 0	Dr Load Char	6th Char	Write 1st Word TI SI	Read Last Word TI SI	Chan Disc	Disc Call		B Cycle Dmd	B Cycle	1st B Cycle	1st BIN Tgr TI			
	TI 30.00	40.02	51.02	DD	20.00	20.00	40.02	20.02	20.11	20.12	20.02	20.01		12.15	12.15	20.06	20.25	20.24	20.23	20.13	20.12		20.03	20.03	20.27	20.27		
		Tape End	1st Char TM TI	End of File TI	Word Par Error	Redun Check	Trans Lass		Prag Ind Sync									Serv Resp		Attn	Attn Resp		Stap	Unus End		End Resp		
		TI 15.00	15.01	15.01	18.02	15.02	20.10		15.04									SI 20.26		SI	SI		SI 20.27	20.29	20.29	SI		
		Enb CWT	Enb TCT Wd Par	Enb Attn		Enb DD Int DD				Attn Sync	Unus End Sync	Wd Par Sync	Disc Sync	Redun Check Sync	EOF Sync				Trop PRI			DD Inter						
		16.00	16.00	SI 16.00		16.00				SI 16.01	16.01	16.01	16.02	16.02	16.02			16.03			DD 51.03							
																		Character Counter										
																		4	2	1								
																		TI SI										
																		17.00	17.00	17.00								

Name	02A1
Name	or
Name	02A2
MFI	(06.XX.YY.1)
Page	

		Assembly Register 1st Character						Assembly Register 2nd Character						Assembly Register 3rd Character												
0 (8)	1 (A)	2 (8)	3 (4)	4 (2)	5 (1)		6 (8)	7 (A)	8 (8)	9 (4)	10 (2)	11 (1)		12 (8)	13 (A)	14 (B)	15 (4)	16 (2)	17 (1)							
11.20	11.20	11.20	11.21	11.21	11.21		11.22	11.22	11.22	11.23	11.23	11.23		11.24	11.24	11.24	11.25	11.25	11.25							
TI SI	TI SI	TI SI	TI SI	TI SI	TI SI		TI SI	TI SI	TI SI	TI SI	TI SI	TI SI		TI SI	TI SI	TI SI	TI SI	TI SI	TI SI							
11.26	11.26	11.26	11.27	11.27	11.27		24 (8)	25 (A)	26 (8)	27 (4)	28 (2)	29 (1)		30 (8)	31 (A)	32 (B)	33 (4)	34 (2)	35 (1)		DR C Bit	Wr T Odd Cnt	Rd Par Gen	DD Stat		
TI SI	TI SI	TI SI	TI SI	TI SI	TI SI		TI SI	TI SI	TI SI	TI SI	TI SI	TI SI		TI SI	TI SI	TI SI	TI SI	TI SI	TI SI		10.12	18.02	18.01	DD 52.00		
3 (4)	4 (2)	5 (1)	6 (4)	7 (2)	B (1)	9 (4)	10 (2)	11 (1)	12 (4)	13 (2)	14 (1)	15 (4)	16 (2)	17 (1)												
12.00	12.00	12.00	12.01	12.01	12.01	12.02	12.02	12.02	12.03	12.03	12.03	12.04	12.04	12.04												
21 (4)	22 (2)	23 (1)	24 (4)	25 (2)	26 (1)	27 (4)	28 (2)	29 (1)	30 (4)	31 (2)	32 (1)	33 (4)	34 (2)	35 (1)												
28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2

02A3
or (06.XX.YY.1)
02A4

Logic Page	Line In	Input*	Channel Line Name	1414-I, II Line Name	Output	Line Out	Logic Page
06.30.01.1	+B	02A3G23B	-C Unit Nu 0 to TAU	-C Unit Nu 0 to TAU	14D1C04A	+S	60.68.50.1
06.30.01.1	+B	02A3G23G	-C Unit Nu 1 to TAU	-C Unit Nu 1 to TAU	14D1C04C	+S	60.68.50.1
06.30.01.1	+B	02A3G23F	-C Unit Nu 2 to TAU	-C Unit Nu 2 to TAU	14D1C04L	+S	60.68.50.1
06.30.01.1	+B	02A3G23E	-C Unit Nu 3 to TAU	-C Unit Nu 3 to TAU	14D1C04B	+S	60.68.51.1
06.30.01.1	+B	02A3G23D	-C Unit Nu 4 to TAU	-C Unit Nu 4 to TAU	14D1C05A	+S	60.68.51.1
06.30.01.1	+B	02A3G23C	-C Unit Nu 5 to TAU	-C Unit Nu 5 to TAU	14D1C05C	+S	60.68.51.1
06.30.01.1	+B	02A3G24B	-C Unit Nu 6 to TAU	-C Unit Nu 6 to TAU	14D1C05L	+S	60.68.52.1
06.30.01.1	+B	02A3G24G	-C Unit Nu 7 to TAU	-C Unit Nu 7 to TAU	14D1C05B	+S	60.68.52.1
06.30.01.1	+B	02A3G24E	-C Unit Nu B to TAU	-C Unit Nu B to TAU	14D1C06A	+S	60.68.52.1
06.30.01.1	+B	02A3G24F	-C Unit Nu 9 to TAU	-C Unit Nu 9 to TAU	14D1C06C	+S	60.68.53.1
06.20.09.1	+B	02A3J01X	-C TAU Write Call	-C Write Tape Call	14D1A20L	+S	60.68.30.1
06.20.09.1	+B	02A3J016	-C TAU Read Call	-C Read Tape Call	14D1A20B	+S	60.68.30.1
06.20.09.1	+B	02A3G22B	-C Backspace Call	-C Backspace Call	14D1A20A	+S	60.68.30.1
06.20.09.1	+B	02A3G22G	-C Write Tape Mark Call	-C Write Tape Mk Call	14D1A20C	+S	60.68.30.1
06.30.00.1	+B	02A3C04B	-C Erase Call to TAU	-C Erase Call	14D1A21B	+S	60.68.31.1
06.20.09.1	+B	02A3G22F	-C Rewind Call	-C Rewind Call	14D1A21A	+S	60.68.31.1
06.20.09.1	+B	02A3G22E	-C Rewind Unload Call	-C Rewind Unload	14D1A21C	+S	60.68.31.1
06.15.00.1	+B	02A1G04D	-C Turn Off Tape Indicate	-C Turn Off Tape Ind	14D1A21L	+S	60.68.31.1
06.19.05.1	+B	02A1J27B	-C Computer Reset to TAU	-C Comp Reset to Tape	14D1A22B	+S	60.68.31.1
06.30.00.1	+B	02A1C15A	-C Write Disc to TAU	-C Disconnect Call	14D1A22A	+S	60.68.32.1
06.20.02.1	+B	02A1C22G	-C Odd Parity Op to TAU	-C Odd Parity Op to TAU	14D1A22C	+S	60.68.32.1
06.30.00.1	+B	02A1H17D	-C Set Tape Select Reg	-C Set Tape Sel Reg	14D1C06B	+S	60.68.53.1
06.20.13.1	+B	02A1F16B	-C Reset Tape Unit Selects	-C Reset Tape Sel Reg	14D1C06L	+S	60.68.53.1
06.11.12.1	+B	02A3J01T	-C Chan Wr Bus 1 to Tape	-C CPU to TAU 1 Bit	14D1A06B	+S	60.68.20.1
06.11.12.1	+B	02A3J01R	-C Chan Wr Bus 2 to Tape	-C CPU to TAU 2 Bit	14D1A06A	+S	60.68.20.1
06.11.12.1	+B	02A3J01C	-C Chan Wr Bus 4 to Tape	-C CPU to TAU 4 Bit	14D1A06C	+S	60.68.20.1
06.11.12.1	+B	02A3J01A	-C Chan Wr Bus B to Tape	-C CPU to TAU B Bit	14D1A06L	+S	60.68.20.1
06.11.12.1	+B	02A3J01Q	-C Chan Wr Bus A to Tape	-C CPU to TAU A Bit	14D1A11B	+S	60.68.21.1
06.11.12.1	+B	02A3J01K	-C Chan Wr Bus B to Tape	-C CPU to TAU B Bit	14D1A11A	+S	60.68.21.1
06.11.12.1	+B	02A3J01F	-C Chan Wr Bus C to Tape	-C CPU to TAU C Bit	14D1A11C	+S	60.68.21.1

Logic Page	Line In	Input	1414-I, II Line Name	Channel Line Name	Output*	Line Out	Logic Page
60.6B.40.1	-S	14D1D0BD	-C TAU to CPU 1 Bit	-C Tape Bit 1	02A3G03X	-B	06.11.01.1
60.6B.40.1	-S	14D1D08C	-C TAU to CPU 2 Bit	-C Tape Bit 2	02A3G03U	-B	06.11.01.1
60.6B.40.1	-S	14D1D0BB	-C TAU to CPU 4 Bit	-C Tape Bit 4	02A3G03P	-B	06.11.01.1
60.6B.40.1	-S	14D1D0BF	-C TAU to CPU 8 Bit	-C Tape Bit B	02A3G03L	-B	06.11.01.1
60.6B.40.1	-S	14D1D07D	-C TAU to CPU A Bit	-C Tape Bit A	02A3G03G	-B	06.11.00.1
60.6B.40.1	-S	14D1D07C	-C TAU to CPU B Bit	-C Tape Bit B	02A3G03D	-B	06.11.00.1
60.6B.40.1	-S	14D1D07B	-C TAU to CPU C Bit	-C Tape Bit C	02A3G03A	-B	06.11.00.1
60.6B.41.1	-S	14D1D05F	-C Tape Error	-C TAU Error	02A1F05K	+B	06.15.02.1
60.6B.41.1	-S	14D1D05C	-C Tape Read Strobe	-C TAU Read Strobe	02A3G022	-B	06.20.26.1
60.6B.41.1	-S	14D1D04B	-C Select at Load Point	-C Tape Select at Loadpoint	02A3D02F	+B	06.20.11.1
60.6B.40.1	-S	14D1D07F	-C Tape Write Strobe	-C TAU Write Strobe	02A3G02U	-B	06.20.26.1
60.6B.41.1	-S	14D1D04D	-C Tape Ready	-C Tape Sel and Rdy from TAU	02A1H10D	+B	06.20.01.1
60.6B.40.1	-S	14D1D05D	-C Write Condition	-C Write Cond from TAU	02A1J15B	+B	06.20.10.1
60.6B.41.1	-S	14D1D04C	-C Select and Rewind	-C Select and Rewind	02A3D02E	+B	06.20.11.1
60.6B.41.1	-S	14D1D04F	-C Select and Tape Ind On	-C Select and Tape Ind On	02A1G0BC	+B	06.15.00.1
60.6B.41.1	-S	14D1D05B	-C Tape Busy	-C TAU Busy	02A3G02A	-B	06.20.12.1

Note

* These overlap channel test points are for channels 1 and 3.

To use these test points for channels 2 and 4, change the chassis locations from 1 to 2 and from 3 to 4. For example:

Channel 1 and 3 test point 02A1J27B or 02A3G23B

is the same as

Channel 2 and 4 test point 02A2J27B or 02A4G23B

1414-I-II-VII **TRIGGER LOCATIONS - TAPE

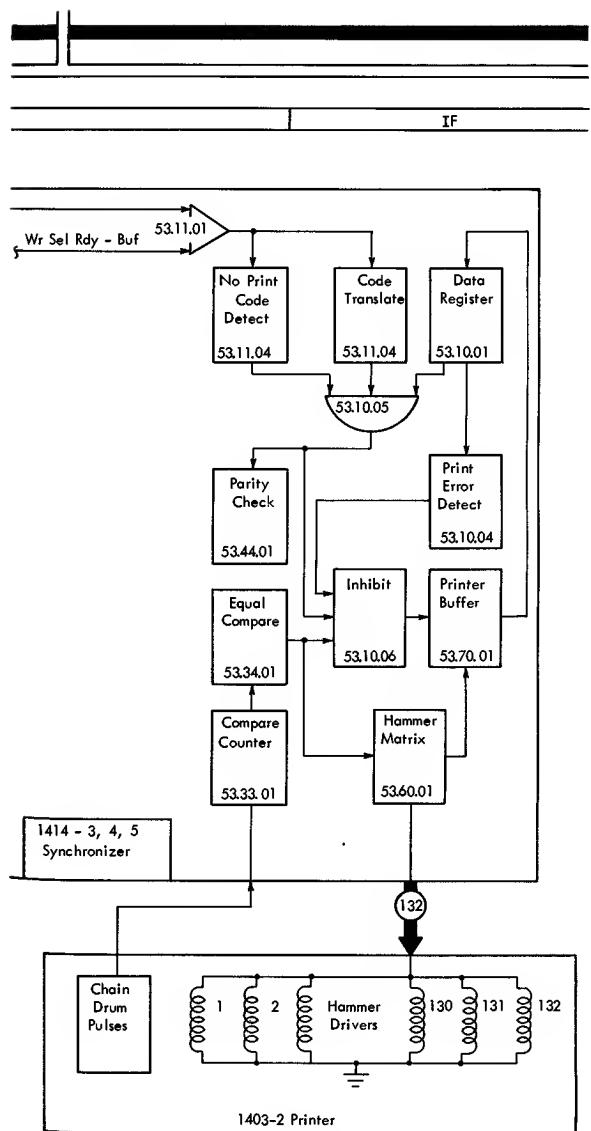
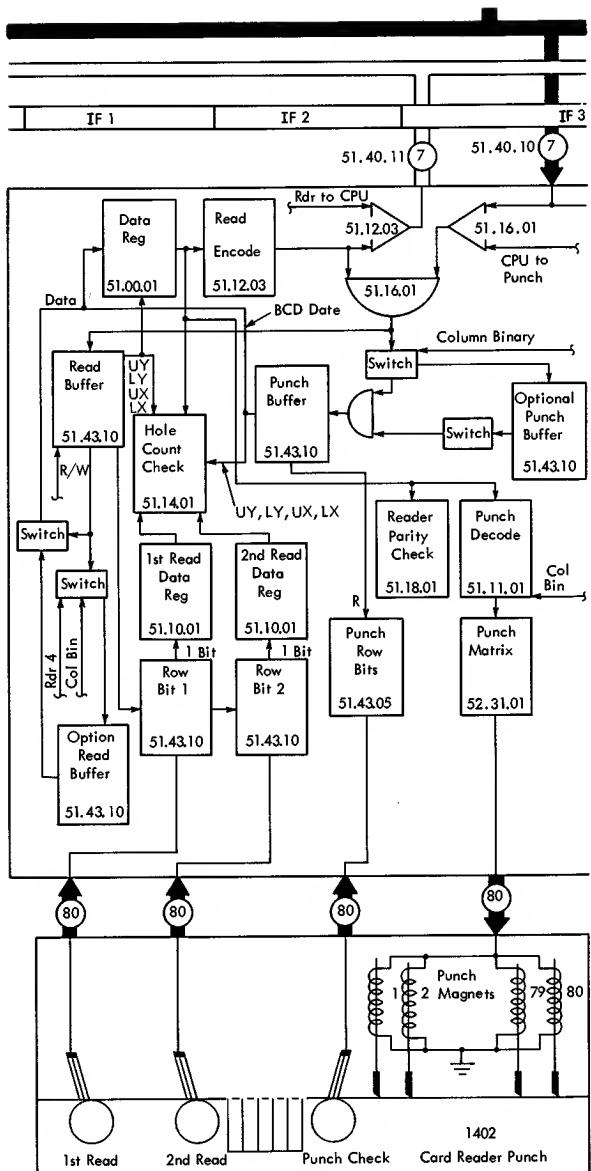
A Reg VRC	60-50-51	R-W Reg 1 Bit	60-40-50
Backspace	60-60-40	R-W Reg 2 Bit	60-40-50
Backward	60-60-40	R-W Reg 4 Bit	60-40-50
Check Character	60-40-61	R-W Reg 8 Bit	60-40-51
Compare Check	60-50-30	R-W Reg A Bit	60-40-51
Disconnect	60-60-31	R-W Reg B Bit	60-40-51
Erase	60-60-31	R-W Reg C Bit	60-40-52
Error Latch	60-50-50	R-W Reg VRC	60-50-50
First Bit	60-40-60	Rewind	60-60-02
First Character	60-40-60	Rewind Unload	60-60-02
Forward Stop Delay	60-30-56	Select Tape Units	60-68-50;53
Gate On Final Amps	60-30-52	Skew Error	60-50-51
Go	60-60-11	Turn On TI	60-60-50
Load Point	60-60-02	Write	60-60-30
No Echo Latch	60-50-50	Write Condition	60-60-30
Odd Redundancy	60-40-61	Write Delay	60-30-11
Read Condition	60-60-20	Write Disc Delay	60-30-11
Read Delay	60-30-10	Write Tgr Release	60-60-31
Read Disc Delay	60-30-10	Write TM	60-60-31
Read Only	60-60-20	CE Switches	60-68-05
		Indicators	60-68-60;62

**For 1414-VII, ALD page numbers start with 90. Thus: 90-XX-XX.

1414-III-IV-VII1 TRIGGER LOCATIONS - CARD

Adv by 2	53-33-05	E O Xfr 1	51-40-12
After 9 CAM	52-10-14	E O Xfer 2	51-40-12
Auto Space	53-55-01	Emitter Delay	53-52-02
Block Data Reg	51-50-01	Equal Compare	53-10-01
Brush SS Litch	52-10-10	Error PT	55-10-06
Buff Full PT	55-10-02	Fast or Slo Skip	53-54-01
Busy Ctl PT	55-10-01	*Five Ring 1-5 Prt	53-21-01
Busy PT	55-10-02	Five Ring Adv	53-23-02
Carriage Moving	53-55-03	Form Check	53-42-01
CB A-1	52-20-02	*Hammer Check Reg	53-10-01
CB Litch	52-10-10	Hammer Row Bit Reg	53-10-02
CCC Reg A-1	53-50-01	Holdover 132	53-40-02
*CE Check	51-14-01	*Home, Printer	53-22-01
CE GO	51-50-03	Indicator Ch 9	53-56-01
CE Reader Rdy	52-11-01	Indicator Ch 12	53-56-01
Chain Home	53-30-01	Insert C Bit	53-11-05
Channel 12-7	53-53-01	*LX Data Reg	51-10-01
Channel 6-1	53-53-02	*LY Data Reg	51-10-01
Clock 000-100	51-30-03	Man Reg Rst	53-50-02
Clock Check	51-30-01	Man Reg Space	53-50-02
*Clock Error	51-30-01	Multi-Rd Fd Latch	52-10-08
Compare A	53-33-03	No Xfr	51-40-12
Compare B	53-33-03	Parity 1	51-18-01
Compare 8	53-33-02	Parity 1 Prt	53-44-02
Compare 4	53-33-02	Parity 2	53-44-01
Compare 2	53-33-01	Parity 2 Prt	53-44-02
Compare 1	53-33-01	PCH Check 1	52-12-02
Ctl Bit Serial	51-50-05	PCH Check 2	52-12-02
*Data Reg A-1 Int Buff	51-10-02	PCH FD	52-10-15
*Data Reg A Prt Buff	53-10-01	PCH Priority Request	52-10-01
*Data Reg B Prt Buff	53-10-01	PCH Data Reg	51-10-01
*Data Reg C Prt Buff	53-10-01	PCH Request	52-10-15
*Data Reg 8 Prt Buff	53-10-02	*PCH SCN	52-10-02
*Data Reg 4 Prt Buff	53-10-02	PCH SCN CB Latch (2F&3J)	52-10-14
*Data Reg 2 Prt Buff	53-10-02	PCH Stack Sel	52-13-01
*Data Reg 1 Prt Buff	53-10-02	Punch FD	52-10-14
Data Reg A-1 PT	55-10-03	PCH Xfr	52-10-15
Delay Forms	53-51-06	PCH Xfr Check	52-12-01
Delay Latch	53-23-03	Print Error	53-12-01
Delay Rst	53-55-03	Print in Process	53-51-06
E O File	52-11-01	*PRT Line Complete Reg	53-10-01
E O File Dly	52-11-01	PS 1-32	53-32-01
*E O Scan	51-32-01	PSS 1	53-31-01

PSS 2	53-31-01	Start Latch CE	51-50-03
PSS 3	53-31-01	Stop Latch CE	51-50-03
PSS Tgr	53-30-01	Strobe	51-40-43
Rd Fd	52-10-09	Strobe Pls Int Buff	51-30-05
Rd Fd Litch	52-10-08	Switch Bounce	53-42-01
Rd Pls 1 Int Buff	51-30-05	Sync Chck	53-43-01
Rd Pls 2 Int Buff	51-30-05	Sync Ctl 1	55-10-01
Rd Priority Request	52-10-01	Sync Ctl 2 Pt	55-10-01
Rd Request	52-10-07	Sync Holdover	53-12-01
Rd Request PT	55-10-06	*Ten Ring 0-7	51-32-01
*Rd Scn	52-10-02	*Ten Ring 0-4 Prt	53-20-01
Rd Scn PT	55-10-07	*Ten Ring 5-9 Prt	53-20-02
Rd Xfr Req PT	55-10-06	Ten Ring AC	51-32-02
Rd Xfr Request	52-10-09	Ten Ring Adv Prt	53-23-02
Rdy Print	53-40-01	*Three Ring 1 Prt	53-22-01
Ready	51-40-04	*Three Ring 2 Prt	53-22-01
*Read Check	52-12-01	*Three Ring 3 Prt	53-22-01
Read In, Prt	53-40-01	Three Ring Adv Prt	53-23-02
Read Request	51-40-01	Time Pls 1	51-30-02
Ring Check Tgr	51-32-02	Time Pls 2	51-30-02
Ring Err 1	51-32-02	Turn Off Rings	53-23-01
*Ring Err 2	51-32-02	*Unit Ring 0-9	51-31-01
Scan Call, Prt	53-40-01	*Unit Ring Error	51-31-02
Scan Req PT	55-10-07	*UX Data Reg	51-10-01
*Scan, Prt	53-40-01	*UY Data Reg	51-10-01
Serial Scn Latch	51-50-06	*Validity Latch	52-12-02
Single Line	53-42-01	Wr Pls Int Buff	51-30-05
Stacker 1	52-13-02	Z Pls Int Buff	51-30-05
Stacker 2	52-13-02	1st Rd Data Reg	51-10-01
Stacker 4	52-13-01	2nd Rd Data Reg	51-10-01
Stacker 8	52-13-01	1401 CCC Reg Rst	53-50-03
Start Latch	53-42-01	1401 Rd Litch	52-10-08
	51 Col Cd Proceed		52-10-11



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
12															
11															
0															
1															
2															
3							#1								
4								#2							
5									#3						
6										#4					
7											#5				
8												#6			
9															

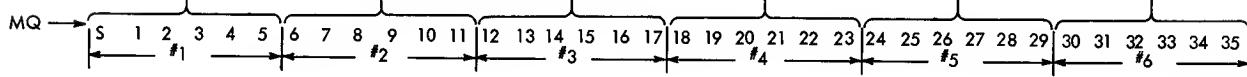
The card is transferred sequentially from column 1 to column 80. This causes the IBM card to be transferred in six column increments. The IBM card fills $13 \frac{1}{3}$ MQ words.

Word

1 1 thru 6
2 7 thru 12
3 13 thru 18
4 19 thru 24
5 25 thru 30
6 31 thru 36
7 37 thru 42

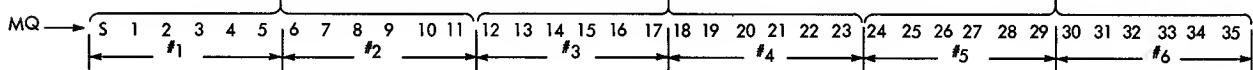
Word

8 43 thru 48
9 49 thru 54
10 55 thru 60
11 61 thru 66
12 67 thru 72
13 73 thru 78
14 79 and 80

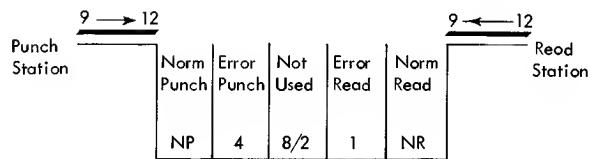
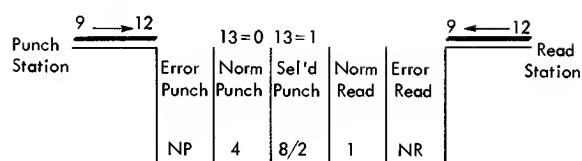


Column	1	2	3	4	5	6	7	8	9	10	11	12	13	
12	S	12	24											
11	1	13	25											
0	2	14	26											
1	3	15	27											
2	4	16	28											
3	5	17	29											
4	6	18	30											
5	7	19	31											
6	8	20	32											
7	9	21	33											
8	10	22	34											
9	11	23	35											

This card is transferred sequentially from column 1 to column 80. This causes the binary card to be transferred in three column increments. The binary card fills $26 \frac{2}{3}$ MQ words starting with column 1 in word 1 positions S, 1, 2, 3, 4, and 5.

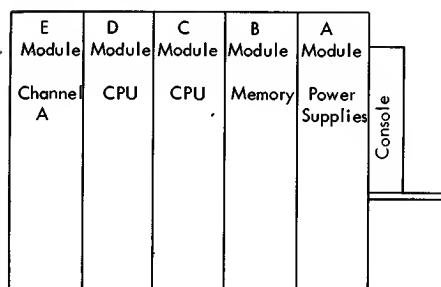


MODULE LAYOUT

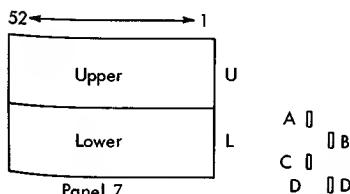
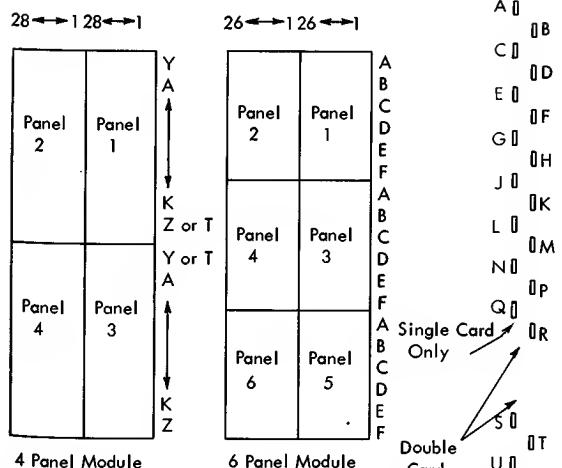


1402 CB and Card Row Relationship

CB	Timing	
9	8 1	C
8	8	
7	4 2 1	
6	4 2	C
5	4 1	C
4	4	
3	2 1	C
2	2	
1	1	
0	A	
11	B	
12	A B C	



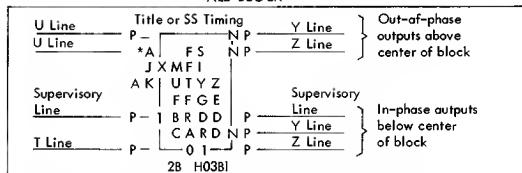
Frame 01



7040 Module Layout Wiring Side

IBM Customer Engineering Component Circuits Reference Card

ALD BLOCK



FS - Functional symbol (up to four characters -A, -TO, SS, ---)
MF1 - Machine feature index or special note (up to four characters)

UT - Line type in

YZ - Line type out

FF - Frame (01 - 99)

G - Sliding gate (A, B, C, D) or module (A, B, C, ---)

E - Engineering change level tag (A, B, C, ---)

B - Chassis (1 - 6) or swinging gate (1 - 8)

R - Chassis Row (A - K) or swinging gate column (A - F)

DD - Chassis column (01 - 28) or swinging gate row (01 - 26)

P - Card socket pin (single cord:A-R; double, Stan-Poc, or twin:A-B)

* A - Edge Connector, Test Point given in Note A

JX - Shield lead connected to pin J (X = twisted pair; * = coaxial cable)

AK - Pin A backplane wired to pin K

CARD - Card code

2B - Page coordinates

H038I - For engineering use; block identification (circuit type)

01 - For engineering use; block configuration (01, 02, 03, ---)

N - When used means normal (not supervisory) output, load in this block.

I - One of six symbols:

3 - Third level input, load in this block

◊ - Third level input, load elsewhere

S - Split level input, load in this block

2 - Split level input, load elsewhere

C - Cascode level input, load in this block

H - Cascode level input, load elsewhere

LINE LEVELS

Line Type	Ideal Swing (volts)	Down Levels (volts)		Up Levels (volts)		Application
		Low	High	Low	High	
B	0 to + 6	+ 0.1	+ 0.3	+2.7	+6.8	DDTL, Uncompensated
B	0 to + 6	+ 0.1	+ 0.3	+5.6	+6.8	DDTL, Compensated
B	0 to + 6	- 0.8	+ 0.8	+3.2	+6.8	DDTL, DE Chain
C	0 to 15 ma	- 4.1	- 0.3	+0.6	+3.1	Std Interface DL, DT
D	-2.5 to +2.5	- 5.0	- 0.7	+0.7	+5.0	DEFL
E	-6 to + 6	- 25.0	- 3.0	+3.0	+25.0	EIA Std Data Sets
N	± from 0 ref	- 3.0	- 0.4	+0.4	+1.2	Alloy Current Sw
N	± from 0 ref	- 0.9	- 0.4	+0.4	+0.6	Diffused Current Sw
P	± from -6 ref	- 7.2	- 6.4	- 5.6	- 3.0	Alloy Current Sw
P	± from -6 ref	- 6.6	- 6.4	- 5.6	- 5.2	Diffused Current Sw
Q	0 to 40 ma	- 3.8	- 0.5*	+0.6	+2.4	DL and DT
R	0 to +12	- 0.4	+ 0.2	+5.6	+12.5	CTRL
S	-12 to 0	-12.5	- 5.6	- 0.2	+0.4	CTRL
S	-12 to 0	-12.5	- 6.9	- 0.5	0.0	SDTRL
S1	-6 to 0	- 6.9	- 5.9	- 0.5	0.0	Clamped SDTDL and SDTRL (7074)
T	-6 to + 6	- 6.2	- 0.7	+1.4	+6.2	CTDL
U	-12 to 0	-12.5	- 7.4	- 5.3	+0.2	CTDL
V	Any					Special
W	# 0 to -48	-53.0	- 43.0	- 2.0	0.0	Relays
X	-30 to +10	-60.0	- 18.3	+5.5	+40.0	Tubes
Y	-6 to 0	- 8.8	- 5.8	- 0.7	- 0.1	SDTDL
Z	-6 to +6	- 7.0	- 4.2	+3.0	+6.2	Magnetic Shift Cores

* High down level can go to +0.1 on some circuits

0 to relay source voltage; typically, 0 to -48

NORMAL PIN ASSIGNMENTS FOR POWER SUPPLY VOLTAGES

Card Type	Gnd	-6v	+6v	-12v	+30v	+12M	-36v	-20v	+6M	+12v	-12M	+20v
All Single	J	K	L	M	N*	N*	P*	P*	Q*	Q*	R	
Double**	J&I	K	L	M	N*	N*	P*	P*	Q*	Q*	R	
Stan-Pac(7104)	1	2	3	4			5		6		8	7
Stan-Pac(7302\$)	J&I		3	4	5*or7		6		5*		8	
Twin#	J&I											

* One of two voltages that may be on this pin

** Current switching circuits (1410, 7030, 7070, 7074, 7080, 7090, 7094)

§ Serial 1200 and above (DEFL circuits)

¶ DDTL circuits (7040, 7044, 7640, 7710, 7750, 7908)

CURRENT SWITCHING SUPERVISORY LEVELS

Line Name	Ref	Down Levels* (volts)			Up Levels* (volts)		
		L	N	H	L	N	H
Third-Level N	0.0	- 2.0	- 1.6	- 1.2	+ 0.4	+ 0.5	+ 0.5
Third-Level P	- 6.0	- 6.5	- 6.5	- 6.4	- 4.8	- 4.4	- 4.0
Split-Level N	0.0	- 2.0	- 1.6	- 1.2	- 0.2	0.0	+ 0.2
Split-Level P	- 6.0	- 6.2	- 6.0	- 5.8	- 4.8	- 4.4	- 4.0
Cascade N (N!)	+ 6.0	+ 5.0	+ 5.3	+ 5.6	+ 6.4	+ 6.5	+ 6.5
Cascade P (P!)	-12.0	-12.5	-12.5	-12.4	-11.6	-11.3	-7.0

* L - Low limit for typical circuits using this line type

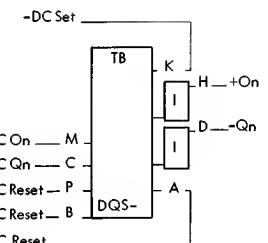
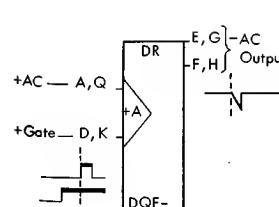
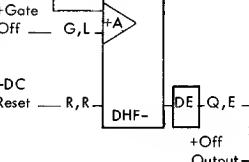
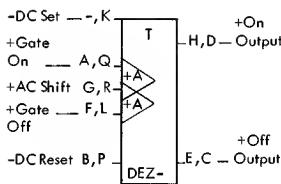
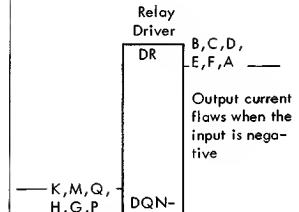
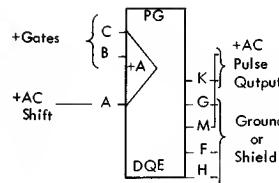
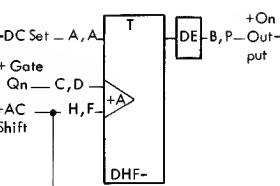
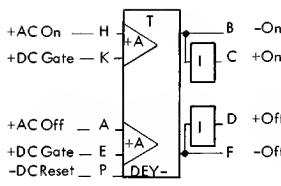
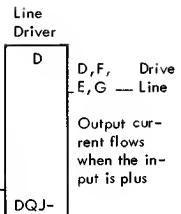
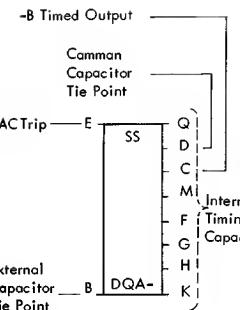
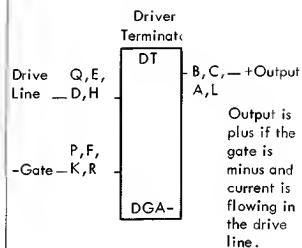
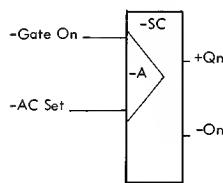
* N - Nominal voltage level

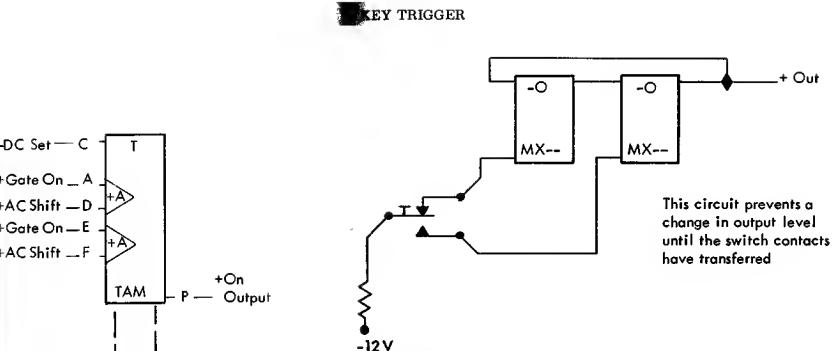
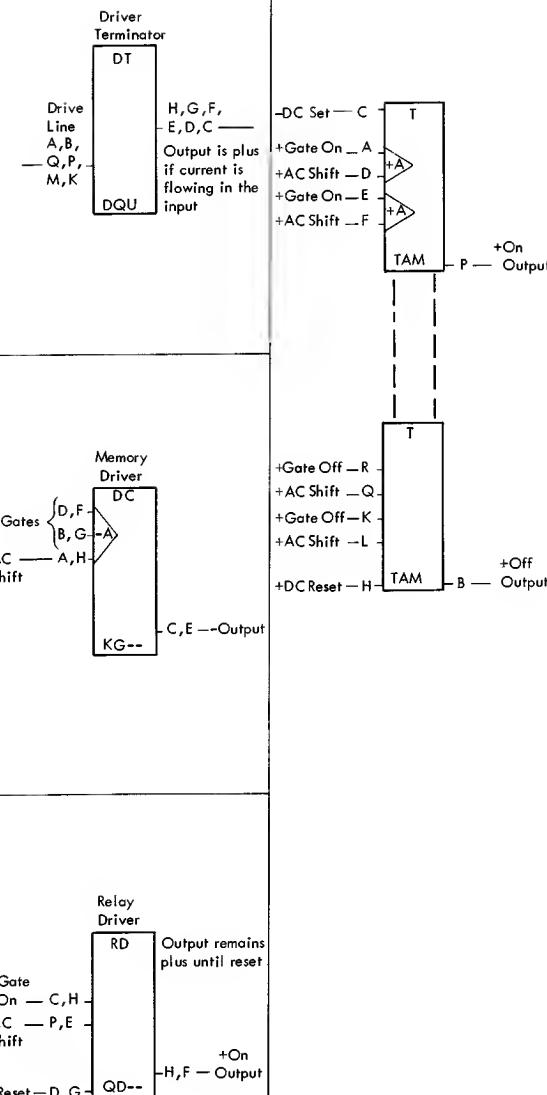
* H - High limit for typical circuits using this line type

7070 SPECIAL CORE DRIVE LEVELS

Line Name	Down Levels (volts)			Up Levels (volts)		
	Low	Nom	High	Low	Nom	High
A Drive (ROD)	+ 1.1	+ 10.0	+ 17.9	+ 28.7	+ 30.0	+ 31.2
B Drive (RID)	- 6.2	- 6.0	- 5.2	+ 12.2	+ 17.0	+ 20.9
B Drive (DRID)	- 5.9	- 5.8	- 5.7	+ 10.8	+ 11.0	+ 11.9
C Drive (ROCD)	+ 6.4	+ 6.4	+ 7.2	+ 11.7	+ 12.0	+ 17.0

LINE DETERMINATION





Key Trigger Circuit

SMS CARDS

P EQUALS POWER SUPPLY CARDS
 * EQUALS 7106 CORE STORAGE CARDS
 ** EQUALS 7107 CORE STORAGE CARDS
 *** EQUALS BOTH 7106 AND 7107 CORE STORAGE CARDS

PART NUMBER	NAME	PART NUMBER	NAME
370697	ANN- *	372126	DPV-
370660	AND- *	372116	DPY-
372188	DB--	372147	DDA-
370659	DLM- *	372140	DBB-
370787	DLP- *	372142	DDC-
370662	DLS- *	372190	DDD-
370786	DLT- *	372144	DDE-
370657	DLU- *	372152	DDF-
370889	DMM-	372150	DDJ-
370890	DMN-	372143	DDM-
370891	DMP-	372151	DDN-
372125	DMD-	372145	DDP-
370892	DMR-	372138	DDR- ***
370893	DMS-	372155	DDS-
370894	DMT-	372148	DDT-
370895	DMU-	372146	DDU-
370896	DMV-	372181	DDX-
370897	DMX-	372233	DXA- *
370898	DMY-	371699	RE-- ***
372103	DNA- **	373102	STZ- *
372105	DNB-	373288	SVR- *
372104	DNC- **	371621	TC-- *
372127	DND-	373295	UCA- ***
372106	DNF-	373301	UCB-
372137	DNH-	373302	UCC-
372164	DNJ- **	373303	UCD-
372163	DNK- **	373304	UCE-
372162	DNL- **	373296	UCF-
372156	DNW-	373297	UCG-
372189	DNY-	373298	UCH-
372261	DNZ-	373312	UCK-
372100	DPA-	373299	UCL-
372124	DPB-	373313	UCM-
372101	DPC-	373350	UCN-
372102	DPD-	373351	UCP-
372107	DPE-	373349	UCD-
372108	DPG-	372187	V7--
372109	DPH-	373101	VJG- *
372110	DPP-	370575	YGA- P
372111	DPO-	370576	YGB- P
372112	DPR-	370579	YGE- P
372113	DPS-	370610	YGH- P
372141	DPT-	370612	YGL- P
372114	DPU-		

DIAGNOSTIC PROGRAMS

HARD CORE TESTS

4HC1A Hard Core Basic Test

1. Load cards 1-13 in BCD card reader
2. Make reader ready--EOF on--START
3. Read select BCD reader in keys
4. RESET - AUTO on - LOAD

For each succeeding card--RESET and LOAD.

Number	Test	Normal	Halt in SR
1	Ones to AC + MQ	HPR	00001
2	Zeros to AC + MQ	HPR	00002
3	Minus Alternates	HPR	00003
4	Plus Alternates	HPR	00004
5	SS 1-2-3 Off	HPR	00005
6	SS 4-5-6 Off	HPR	00006
7	SS 1-2-3 On	HPR	00007
8	SS 4-5-6 On	HPR	00010
9	Keys to ACC		
	IORD to MQ	HPR	00011
10	Typewriter Test	HPR	00012
11	Type: Hard Core Test	HPR	00013
12	Reads Thirteen		
13	Type: Loader OK etc.	HPR	00216

1. Put card 14 before each program deck.
This is a one card BCD load to 1005.
Only one program in the reader at a time.
Decks are full BCD and must be in order.
2. Read select BCD reader in keys.
See Sense Switches listed below.
3. RESET and LOAD.

Following programs have slight changes for use without DCP.

	Error Halt	Normal Halt in SR
HC51A	HPR 51 Adr of Halt	HPR 51 00051
HC52A	HPR 52 Adr of Halt	HPR 52 00052
HC53A	HPR 53 Adr of Halt	HPR 53 00053
HC54A	HPR 54 Adr of Halt	HPR 54 00054
HC55A	HPR 55 Adr of <u>Error</u>	HPR 55 00055

Sense Switches

- 1 on Loop routine
- 2 on Bypass errors
- 3 on HC55 can halt on error
- 4 on HC55 bypass long typeout
- 5 on No effect
- 6 on Repeat program. Type out after 1000 passes.

4HC2A Hard Core Test from Tapes

1. Load 4HC2 tape on any drive on any channel, except 1401 tapes.
2. Read select the tape drive in binary mode in the keys.
3. RESET - AUTO on - LOAD
4. For each succeeding record--RESET and LOAD

Number	Test	Normal	Halt in SR
1	Ones to AC + MQ	HPR	00001
2	Zeros to AC + MQ	HPR	00002
3	Minus Alternates	HPR	00003
4	Plus Alternates	HPR	00004
5	SS 1-2-3 Off	HPR	00005
6	SS 4-5-6 Off	HPR	00006
7	SS 1-2-3 On	HPR	00007
8	SS 4-5-6 On	HPR	00010
9	Keys to ACC		
	IORD to MQ	HPR	00011
10	Typewriter Test	HPR	00012
11	Type: Hard Core Test	HPR	00013
12	Reads Thirteen		
13	Type: Loader OK etc.	HPR	00216

Record 14 is a dummy--needed after each LOAD as LOAD spaces tape.

Fifteen is a loader for hard core versions of CPU diagnostics 51-55.

See Sense Switches listed below.

RESET and LOAD.

Following programs have slight changes for use without DCP.

	Error Halt	Normal Halt in SR
HC51A	HPR 51 Adr of Halt	HPR 51 00051
HC52A	HPR 52 Adr of Halt	HPR 52 00052
HC53A	HPR 53 Adr of Halt	HPR 53 00053
HC54A	HPR 54 Adr of Halt	HPR 54 00054
HC55A	HPR 55 Adr of <u>Error</u>	HPR 55 00055

Sense Switches

- 1 on Loop routine
- 2 on Bypass Errors
- 3 on HC55 can halt on error
- 4 on HC55 bypass long typeout
- 5 on No effect
- 6 on Repeat program. Type out after 1000 passes.

7040-7044 PROGRAMS

Hard Core for CPU

4HC1 Card Version } Both Have
4HC2 Tape Version } HC51, HC52, HC53, HC54, HC55

Diagnostic Control Programs (DCP)

4DC1 for Binary Cards
4DC2 for BCD Cards
4DC3 for Taped Programs

CPU Diagnostics

4M51
4M52
4M53 } Run as a sequenced group.
4M54
4M55

4M56 Extended Performance
4M58 Memory Protect
4M59 Interval Timer
4M61 Single Precision Floating Point
4M63 Double Precision Floating Point

Memory Diagnostics

4S83 Hi } For 8K 8 usec Memory
4S84 Lo }

4S53 Hi } For 16K 8 or 2.5 Memory
4S54 Lo }

4S55 Hi } For 32K 8 or 2.5 Memory
4S56 Lo }

Systems Test

4SY1 16K or 32K Memory
4SY3 8K Memory

Utility

4UT1 Diagnostic Tape Generator
4UT2 1414 Simulator
4UT3 Diagnostic Tape Punch-Out

7040-7044 I-O PROGRAMS

Typewriter

4TY1 Typewriter

Card Machines

4RP2 1402 Reader/Punch
4RP6 1622 Reader/Punch
4PR3 1403 Printer

Channel

4CH1 Basic Overlap Test

Tape Diagnostics

4T51 Basic, Part I
4T52 Basic, Part II
4T55 Gap Tests
4T57 Compatibility

1301/7320 File

4F01 7631 Control Unit Test (Both)
4F09 Format/Home Address Generator (Both)
4F10 1301 Surface Analysis
4DR1 7320 Surface Analysis

1401 Diagnostics

4C51 7040/44 to 1401 Interface
4C52 1401 Answer-Back
For 4C51 and 4SY1
4C53 Small 1401 Answer-Back
For 4C51 and 4SY1

Remote Inquiry Typewriter

4MQ1 Diagnostic

Paper Tape

4PT1 Channel A Only
4PT3 Overlap Channels Only

Direct Data

4C55 Master Program
4C56 Slave Program

LOAD AND GO

From Binary Cards

1. Load 4DC1 in the card reader with other desired binary decks following.
2. EOF on - START.
3. Set panel keys to +0762 030 01230.
4. RESET - AUTO on - LOAD

Halt 00000 will display contents of 472 in the Acc and contents of 471 in the MQ. If the configuration words displayed are not correct, set AUTO off and manually load locations 472 and 471 with configuration words 1 and 2 respectively.

5. AUTO on - START

From BCD Cards

1. Load 4DC2 in the card reader with other desired BCD decks following.
2. EOF on - START.
3. Set panel keys to +0762 030 01210.
4. RESET - AUTO on - LOAD.

Halt 00000 will display contents of 472 in the Acc and contents of 471 in the MQ. If the configuration words are not correct, set AUTO off and manually load locations 472 and 471 with configuration words 1 and 2 respectively.

5. AUTO on - START.

From DCP Binary Tape

1. 4DC3 will be on the prepared tape.
2. Load tape on desired channel on tape unit 1.
3. Set proper RDS in the panel keys - +0762 000 XXXXX.
For channel A, XXXXX equals 1221.
For channel B, XXXXX equals 2221.
For channel C, XXXXX equals 3221.
For channel D, XXXXX equals 4221.
For channel E, XXXXX equals 5221.
4. Change prefix in keys from +0 to -0.
5. Turn on Sense Switch 5.
6. RESET - AUTO on - LOAD.

Halt 00000 will display contents of 472 in the Acc and contents of 471 in the MQ. If the configuration words displayed are not correct, set AUTO off and manually load locations 472 and 471 with configuration words 1 and 2 respectively.

7. Release Sense Switch 5.
8. AUTO on - START.

CONFIGURATION WORD 1-472		CONFIGURATION WORD 2-471	
BIT	DEFINITION	BIT	DEFINITION
1	1402 RDR/PCH-INTERFACE 3	5	1011 PAPER TAPE-CHANNEL A
2	1403 CDR/BIN-INTERFACE 3	6	SPARE
3	1403 PRINTER-INTERFACE 3	7	SPARE
4	1402 RDR/PCH-INTERFACE 1	8	SPARE
5	1403 PRINTER-INTERFACE 1	9	SPARE
6	1402 RDR/PCH-INTERFACE 2	10	1009 DATA TRANS-CHANNEL A
7	1403 CDR/BIN-INTERFACE 2	11	1009 DATA TRANS-CHANNEL B
8	1403 PRINTER-INTERFACE 2	12	1009 DATA TRANS-CHANNEL C
9	1403 DN CHANNEL A	13	1009 DATA TRANS-CHANNEL D
10	1622 RDR/PCH	14	1009 DATA TRANS-CHANNEL E
11	1014 REMOTE INQUIRY	15	USED WITH CONF.REQ.HDRD FOR
12	DIRECT DATA INTERFACES	16	THE 7750/7740/7440 PROGRAM
13	CYLINDER MODE ON FILES	17	7750/7740/7440--CHANNEL B
14	1301 FILE ON CHANNEL A	18	7750/7740/7440--CHANNEL C
15	1301 FILE ON CHANNEL E	19	7750/7740/7440--CHANNEL D
16	1301 FILE ON CHANNEL D	20	7750/7740/7440--CHANNEL E
17	1301 FILE ON CHANNEL C	21	7750/7740/7440--CHANNEL A
18	1301 FILE ON CHANNEL B	22	SHARED FILE
19	DIRECT DATA DN CHAN-E	23	SPARE
20	DIRECT DATA DN CHAN-D	24	SPARE
21	DIRECT DATA DN CHAN-C	25	SPARE
22	DIRECT DATA DN CHAN-B	26	SPARE
23	TAPEs AVAILABLE-CHAN-E	27	SPARE
24	TAPEs AVAILABLE-CHAN-D	28	SPARE
25	TAPEs AVAILABLE-CHAN-C	29	SPARE
26	TAPEs AVAILABLE-CHAN-B	30	SINGLE PRECISION F.P.
27	TAPEs AVAILABLE-CHAN-A	31	INTERVAL TIMER-16 MILLISEC.
28	INTERVAL TIMER-16 F.P.	32	INTERVAL TIMER-1 MILLISEC.
29	SINGLE PRECISION F.P.	33	NEED FILE-----CHANNEL A
30	INTERVAL TIMER-16 MILLISEC.	34	NEED FILE-----CHANNEL B
31	EXTENDED PERFORMANCE	35	NEED FILE-----CHANNEL C
32	4 K MEMORY SIZE	36	NEED FILE-----CHANNEL D
33+4-00	4 K MEMORY SIZE	37	NEED FILE-----CHANNEL E
33+4-01	8 K MEMORY SIZE		
33+4-10	32 K MEMORY SIZE		
33+4-11	32K MEMORY SIZE		
35-0	8.0 MICROSECOND STDRAGE		
35-1	2.5 MICROSECOND STDRAGE		

Notes

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